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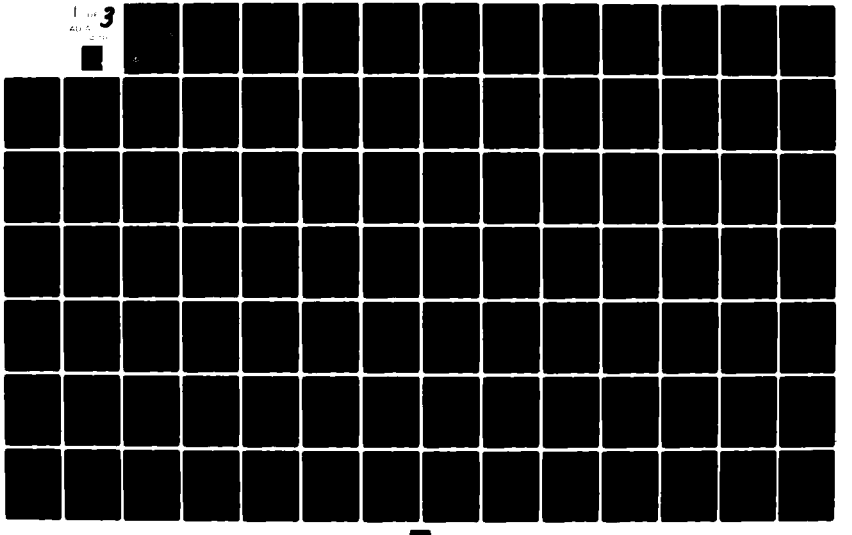

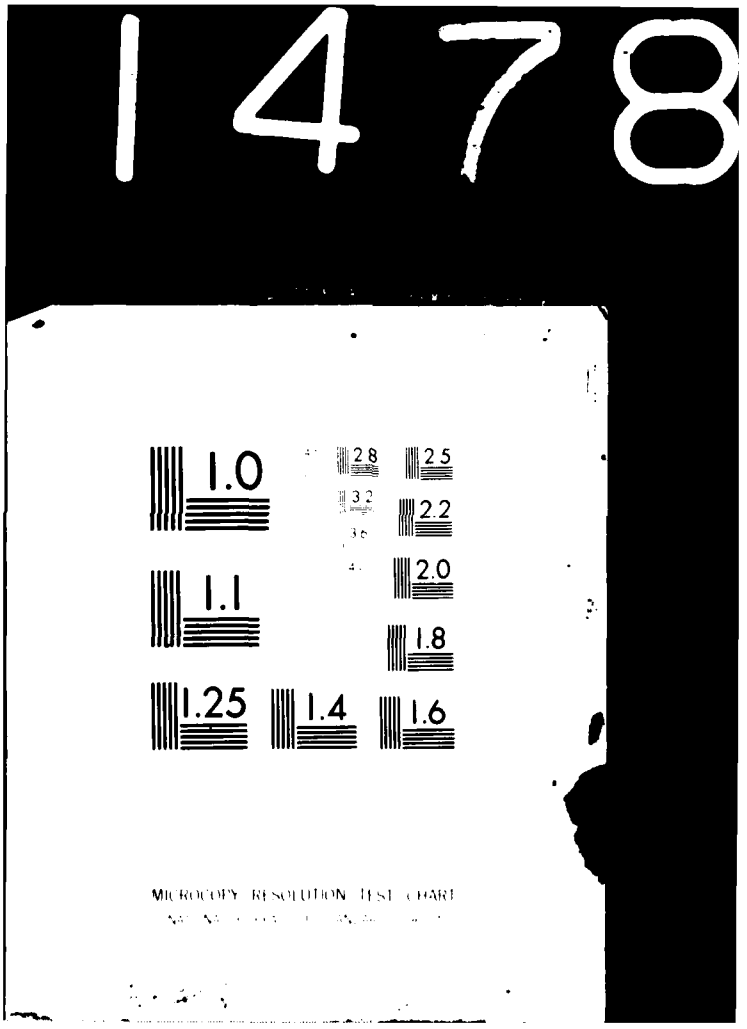
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MICROCOPY RESOLUTION TEST CHART

NSWC TR 80-433

OUTPUT SIGNAL CONDITIONER BASIC HARDWARE DESCRIPTION

BY JAAN A. LAANISTO

UNDERWATER SYSTEMS DEPARTMENT

1 OCTOBER 1980

NAVAL SURFACE WEAPONS CENTER

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Output Signal Conditioner Basic Hardware (OSCBH) was designed to provide digital to analog conversion of simulated data generated by the Digital Acoustic Sensor System (DASS), and a high speed Random Number Generator to be used by the simulation algorithms in the AN/UYS-1. Details concerning the design, construction and testing of unit are given in this report.

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FOREWORD

The Output Signal Conditioner Basic Hardware (OSCBH) was designed and constructed to provide certain capabilities for the Digital Acoustic Sensor Simulator (DASS) (Figure 1). The DASS System utilizes two processors to provide a two stage simulation system. An AN/UYK-20 minicomputer is used as a preprocessor which accepts user modeling parameters and converts them into a form to be input to the second processor which generates the simulated wave forms. The second processor used is the AN/UYS-1 which is a high speed programmable processor controlled by a general purpose computer. The OSCBH is interfaced to the AN/UYS-1 to provide two major functions, a means of converting simulated sonobuoy analog waveforms from the stored waveforms in the AN/UYS-1 and a high speed random number generator to be used by the simulation algorithms in the AN/UYS-1.

T. B. Hanrahan

F. B. SANCHEZ
By direction

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CHAPTER 1

HARDWARE REQUIREMENTS

The capabilities provided by the OSCBH for the DASS are:

a. 24 Digital to Analog (D/A) channels sampling a software defined data area in AN/UYS-1 memory

b. high speed generation of pseudo-random number sequences to be stored into a software defined area in AN/UYS-1 memory

c. an interrupt generating active ping recognition capability

d. software accessible control and status registers within the OSCBH.

After examining the interface alternatives offered by the AN/UYS-1, several conclusions were made. The first conclusion was that the high data rate required by the OSCBH and the AN/UYS-1 software to execute the simulation algorithms precluded use of the PROTEUS Input/Output Channels (PDC). The second conclusion was that the Input Signal Conditioner (ISC) subunit in the AN/UYS-1 would not be utilized by the DASS simulation algorithms and could therefore be removed. An analysis of the interfacing available between the AN/UYS-1 and the ISC revealed that the OSCBH could replace the ISC. The data busses available in the AN/UYS-1 were the Error Correcting Data Bus (ECDB) and the External Data Bus (EDB). The ECDB allows transfer of data to and from memory at an acceptable rate to meet requirements with the critical write cycle being one 32-bit data word in 400 nano seconds or at a rate of 2.5 MHz. The EDB provides a means of transferring control and status information to and from the OSCBH. In addition to the data busses, an interrupt (ISC interrupt) line and power were available to the OSCBH. The main disadvantage to using the ISC slot was the possible complications caused by extending these two busses (ECDB and EDB) five feet to the OSCBH. After weighing all the advantages and disadvantages, the ISC was selected to provide the means of interfacing the OSCBH to the AN/UYS-1.

With the interface requirements defined by the AN/UYS-1, a specific set of OSCBH design requirements was developed for implementation. The detailed requirements will be enumerated below covering both the software (external register addresses for parameters) and hardware requirements.

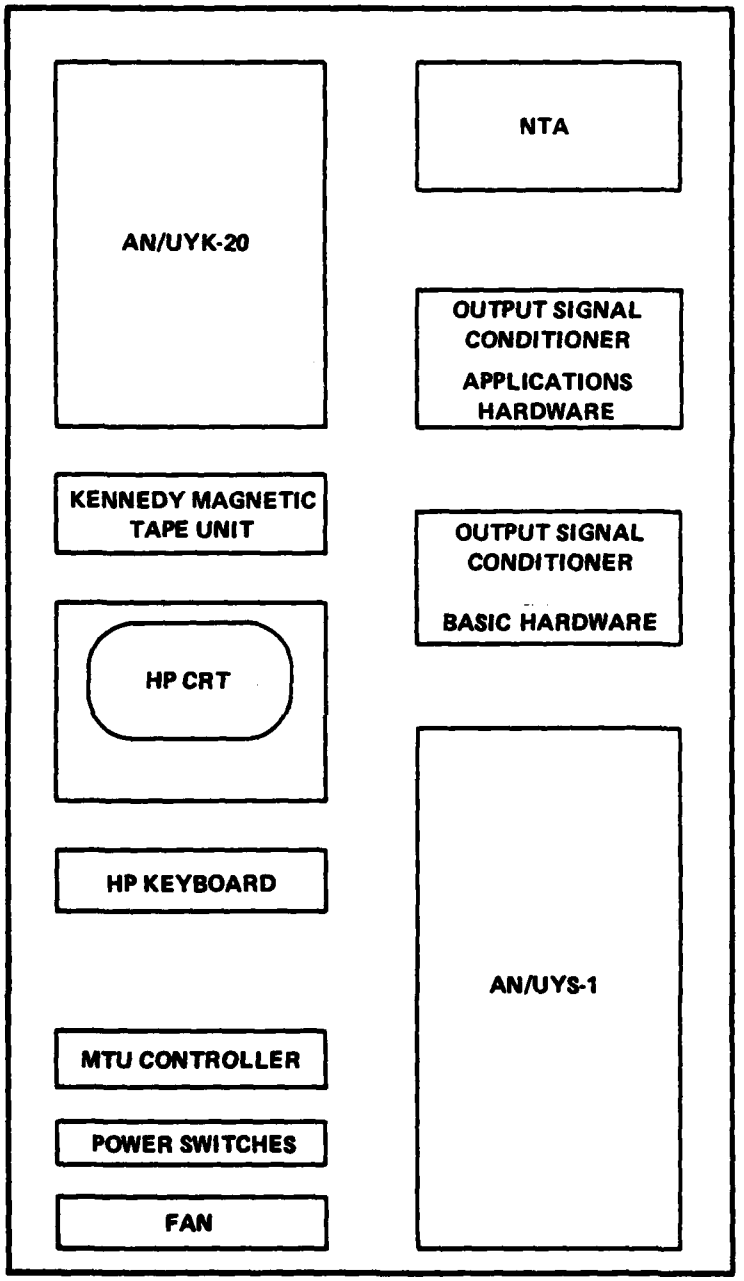


FIGURE 1 DASS CONFIGURATION

DIGITAL-TO-ANALOG CONVERTERS

The Digital-to-Analog converter section has a total of 24 separate channels. The digital information to be converted is contained in Bulk Store (BS) memory of the AN/UYS-1. It consists of one contiguous block of Bulk Store memory. This area of memory is then broken up into smaller blocks in which each block represents a D/A channel (Figure 2). Each Bulk Store location is made up of one 64-bit double word. This 64-bit word is then subdivided into either four 16-bit samples or eight 8-bit samples depending on the mode requested by the user.

A programmable Real Time Clock (RTC) is included to provide a user defined sampling frequency for the D/A converters. The basic clock frequency was selected to be 2 to 21st power times 3 Hz (6.291456 MHz) with an accuracy of $\pm$ .005% and crystal controlled. This basic frequency is to be divided by a 16-bit interval parameter to generate a RTC pulse rate of 6291456 pulses per second (interval parameter equals 1) to approximately 96 pulses per second (interval parameters equals 65535). The 16-bit interval value is converted into the divisor by the following relationship:

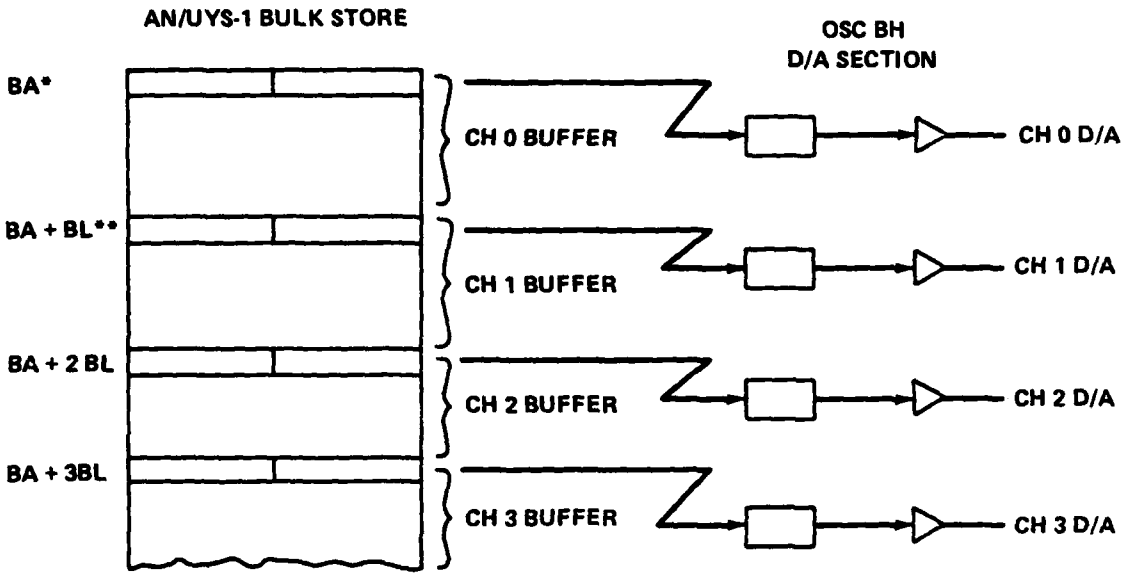
$$X = N_0 (256N_1 + 16 N_2 + N_3)$$

where X is the final divisor, N_0 is bits 0 - 3, N_1 is bits 4 - 7, N_2 is bits 8 - 11 and N_3 is bits 12 - 15. The fundamental sampling frequency chosen for simulation is 6144 samples per second which corresponds to a RTC interval value of either 4100_H or 1400_H.

Each D/A converter is double buffered so that any delay in accessing Bulk Store will not cause a loss of data (data dropouts). The updating circuitry is designed to allow the maximum number of channels (24) to be updated within .5 micro-seconds in order to provide a simultaneous update on all channels relative to the simulated waveform frequency. The accuracy of the waveform requires a 12-bit monotonic digital-to-analog converter with a dynamic range of $\pm$ 5 volts.

A set of programmable parameters is defined to allow the AN/UYS-1 software to configure the OSCBH digital-to-analog converter section to a particular Bulk Store memory configuration. These parameters are the Bulk Store Initial Address (defining the beginning address of the D/A block), number of D/A channels active in the OSCBH, length of a D/A channel block in Bulk Store and the Real Time Clock Interval. The four parameters are transferred to the OSCBH over the 16-bit External Data Bus.

An important requirement for any waveform simulation is to provide continuous waveforms without any breaks. A first step is to provide either a means of automatically recycling the D/A section or issuing an interrupt to the AN/UYS-1 and having the software restart the D/A's. In any case, an interrupt notifying the AN/UYS-1 that the BS buffer has been exhausted and new data should be loaded was found to be a necessary requirement. The time necessary to field the interrupt, reload the D/A Bulk Store block and transfer the parameters over the EDB bus was determined to require too much processor time. A compromise technique was used in which an interrupt is issued to the AN/UYS-1 to update



* BA = D/A BASE ADDRESS
** BL = D/A BUFFER LENGTH

FIGURE 2 D/A BUFFER CONFIGURATION

bulk store memory while the OSCBH automatically reloads its parameters and starts a new cycle. To further preclude data dropouts the D/A section of the OSCBH was assigned a higher priority than Random Number Generator. This will be expanded in a later section.

In addition to the D/A converter, a low-pass filter is also required to correct for the sin x/x attenuation of the Digital-to-Analog Converter from dc to 2.5 KHz. The filter and other specifications for the filter are found in Appendix A. Due to the space limitations in the OSCBH enclosure, the sin x/x filters were designed into the OSC Applications Hardware enclosure.

RANDOM NUMBER GENERATOR

The Random Number Generator (RNG) section of the OSCBH is required to provide the following characteristics:

a. Generate a 32-bit uniformly distributed random number every 400 nanoseconds.

b. Generate 2 16-bit Gaussian distributed random numbers every 400 nanoseconds.

c. Generate 4 8-bit Gaussian distributed random numbers every 400 nanoseconds.

(The 400 nanoseconds constraint is imposed by the AN/UYS-1 ECDB requirement for transferring a 32-bit word.)

Three parameters are required to be transferred to and from the OSCBH. As with the D/A section, the initial Bulk Store address and block size are required to be loaded into the OSCBH. The third parameter is the Random Number Generator 39-bit seed which can be either loaded into the OSCBH or read by the AN/UYS-1. This feature allows the simulation software to generate and store a continuous set of random numbers.

The RNG section of the OSCBH will not generate an interrupt to the AN/UYS-1 when it has finished generating the requested amount of random numbers. Instead, a bit in the status word will be used to signify if the RNG is busy.

Finally, because the D/A section requires top priority, the random number generator must have a provision to be interrupted by the D/A section or hold off activation until the D/A section relinquishes control of the OSCBH.

ACTIVE PING RECOGNITION

This feature was added to provide the means of simulating a DICASS buoy. Ping trigger inputs to the OSCBH are provided which generate an interrupt when any of the four ping trigger inputs are toggled. The RF channel of the trigger input is stored into the status word of the OSCBH and then the status word is read by the AN/UYS-1 in response to the interrupt.

STATUS AND CONTROL

In addition to the parameters given in the D/A and RNG, two additional registers are required: a status register and a mode register. As with the other parameters and/or registers previously discussed, these registers must be accessible over the EDB. The OSC status register provides the status of the OSCBH. The information provided by the register is the source of the interrupt (D/A or Ping trigger), RNG status (busy or not busy), and any errors encountered in transferring data over the ECDB (illegal Bulk Store Address, Double ECC error or ECDB parity error). The mode register is used in two ways: activation of an OSCBH subsection (i.e., D/A and/or RNG) and operating mode of each subsection (i.e., 8-or 16-bit D/A samples).

CHAPTER 2

MODULE DESCRIPTION

The Output Signal Conditioner - Basic Hardware (OSCBH) configuration is presented in Figure 3. The circuitry has been divided into six basic modules,

a. External Data Bus/Real Time Clock

b. Bulk Store Address Generation

c. Random Number Generator

d. Digital-to-Analog Converters

e. Basic Hardware Control

A. EXTERNAL DATA BUS/REAL TIME CLOCK (EDB/RTC). This module interfaces to the EDB of the AN/UYS-1 and is responsible for generating all timing sequences for that bus. The EDB bus operation can be found in Ref. 1, and is reproduced in this report as Figure 4. OSC External Register Addressing decode and strobe circuitry is located in this section. A word counter is also implemented in conjunction with the decoding circuitry for generating consecutive word count pulses for transferring the parameters shown in Table 1. Parity generation and checking for the EDB bus is also located in this module. The programmable Real Time Clock is located in this module and is used to provide the sampling pulses for the D/A module (to be described later). The real time clock interval is software programmable by the AN/UYS-1, refer to Table 1.

B. BULK STORE ADDRESS GENERATION. This module contains the bulk store address generation logic for the D/A and RNG modes of the OSCBH. Figure 5 shows the subdivisions of the modules. Figure 5 is broken down into the two Augat circuit cards, BSAG1 and BSAG2. Also included in this programare the buffers and registers corresponding to the A/D hardware which was not required in this system configuration. All the parameters transferred to the OSCBH to the Bulk Store Address Generator are double buffered to prevent data dropouts. The address generation is performed in two ways, depending on the mode of operation the OSCBH is selected.

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[1]IBM, "Proteus Analyzer Unit Final Maintenance Manual," IBM 76-539-001, pg. 3-368.

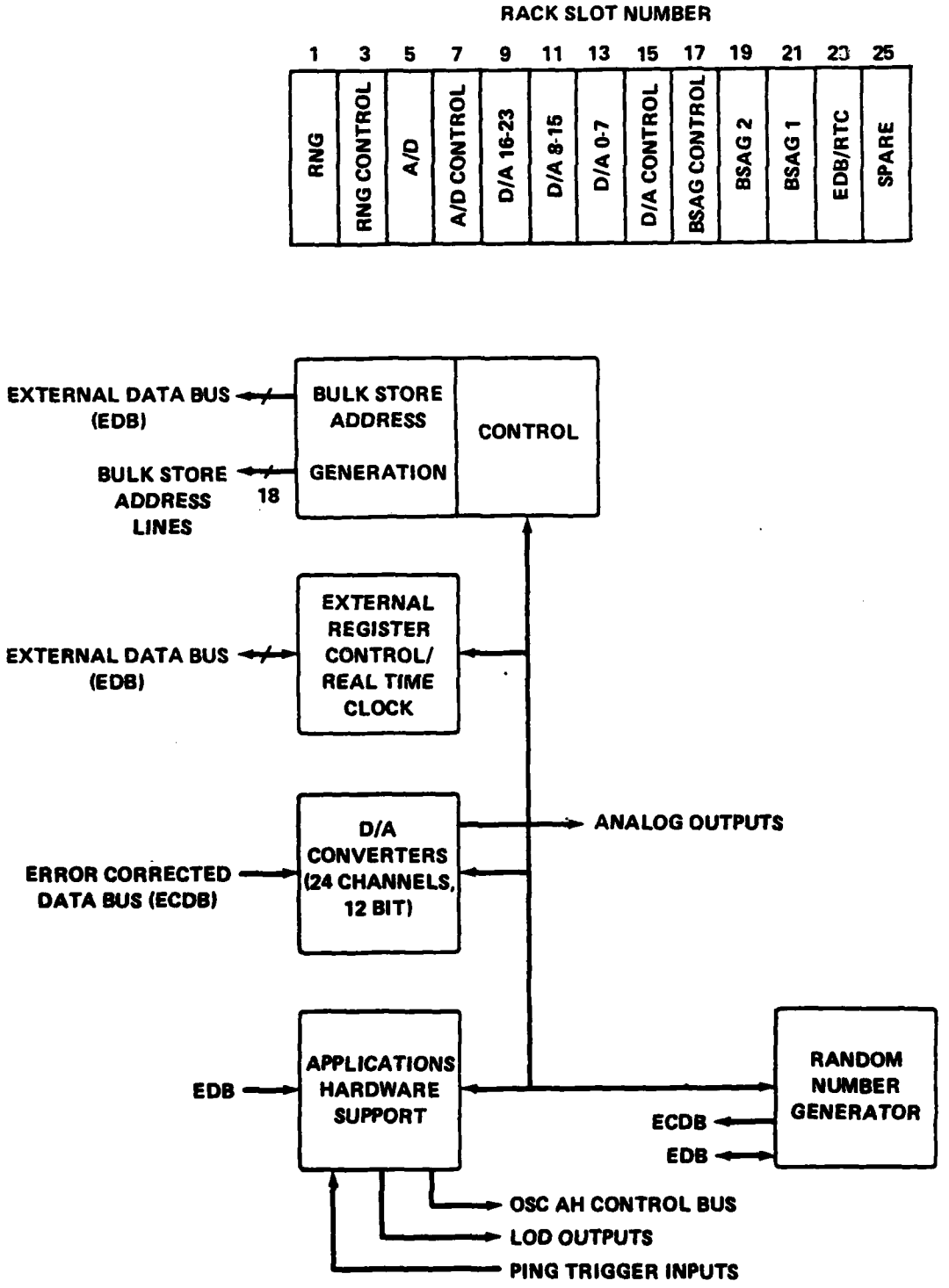
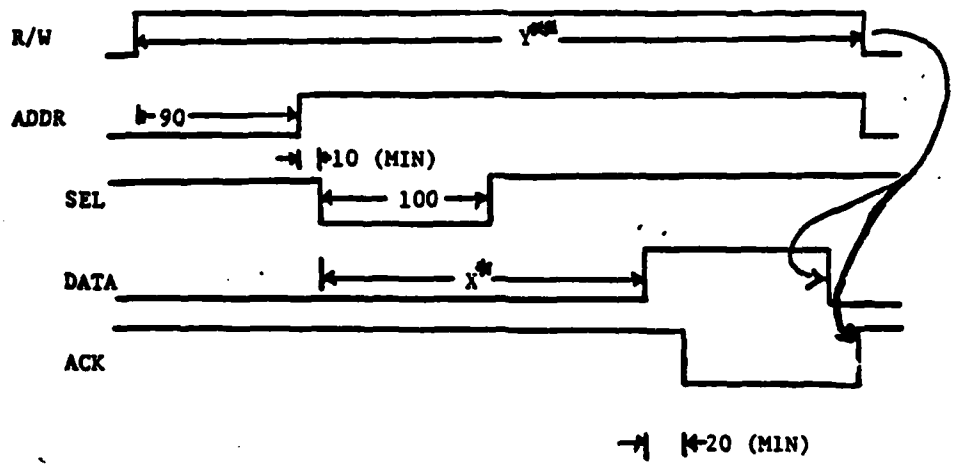


FIGURE 3 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE BLOCK DIAGRAM

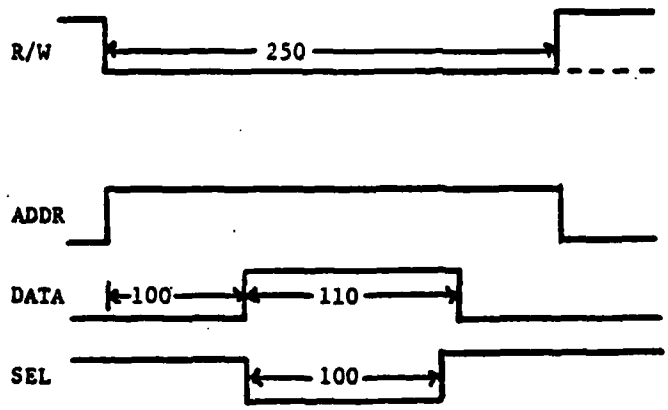
READ TIMING (AT EXTERNAL REGISTER)



*For minimum CP cycle, X ≤ 150ns (Note: Time from Tristate driver gate signal to output onto EDB is 80ns; thus, gate signal must follow select by 70ns for minimum CP cycle).

**For X < 150ns, Y = 350ns (Y increases in 100ns increments; e.g., 150ns < X ≤ 250ns, Y = 450ns).

WRITE TIMING (AT EXTERNAL REGISTER)



Deskewing of SEL and DATA must be performed by external register or trailing edge of SEL used as strobe.

FIGURE 4 EXTERNAL BUS TIMING

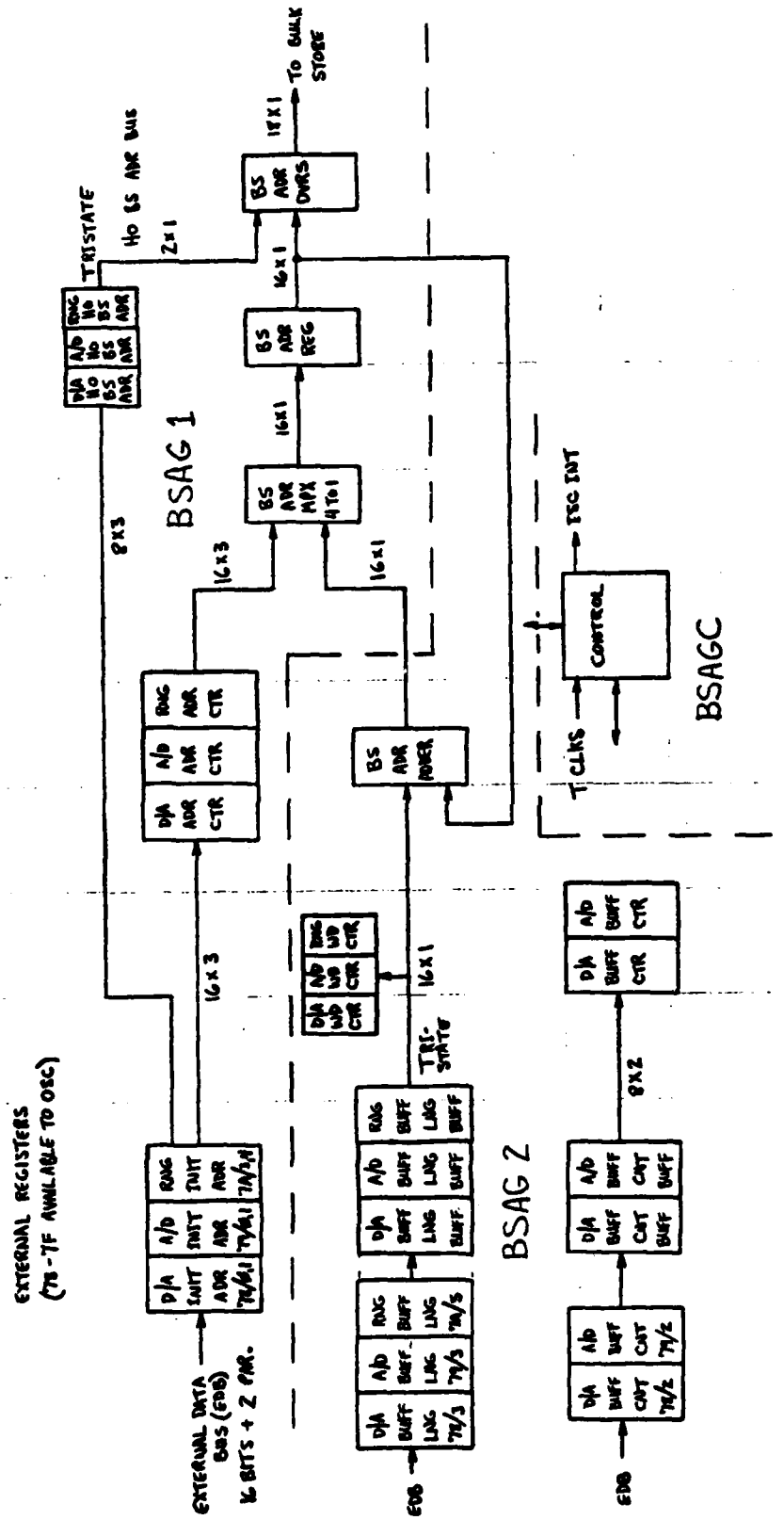


FIGURE 5 OSC OPERATING PARAMETERS AND BULK STORE ADDRESS GENERATION

In the D/A mode, addresses are generated by first loading the initial address into the BS ADR REG which points to the first D/A channel in Bulk Store. After this double word is received, the contents of the BS ADR REG is added to the contents of the D/A Buffer Length Buffer to address the same element in 2nd D/A buffer in Bulk Store. This procedure is then repeated until the buffer counter (number of D/A channels) has counted down to zero. At this point the D/A WD CTR (Word Counter) is decremented by one indicating that all the channels have been updated. When the D/A WD CTR (D/A Word Counter which keeps track of the data words read from any one D/A buffer) decrements to zero, the D/A BUFF LENGTH BUFF and the D/A BUFF CNT BUFF are loaded from their respective registers to begin the count again. Also the initial address is loaded into the D/A ADR CTR from the D/A INIT ADR REG allowing the D/A sequence to begin at the initial location in the new D/A Bulk Store buffer.

The addressing sequence for the RNG mode utilizes only the RNG WD CTR and the RNG buffer length is loaded from the RNG BUFF LNG BUFF into the RNG WD CTR. The operation of the RNG only requires incrementing the address counter through a contiguous area in memory until the RNG WD CTR counts down zero. At the end of the block, the RNG address logic shuts down until a new request is made with a new set of address parameters. This operation is only performed on demand.

C. RANDOM NUMBER GENERATOR. The Random Number Generator (RNG) was incorporated into the OSCBH as a completely separate unit with the RNG operated via the control logic of the OSCBH. Figure 6 shows the architecture of the RNG (the implementation design will be discussed in a later section). Because this module only incorporates the random number generator, no addressing or counting capabilities are included (this function is performed in the previous section). To generate random numbers, the RNG module has a programmable 39-bit register (Main Reg in Figure 6) from which a block of random numbers are to be generated. After a block of random numbers have been generated, the final value in the Main Register can then be read over the EDB by the AN/UYS-1. By reloading the RNG with this value a new block of data can be generated which would be continuous with the previous block. To transfer random numbers to AN/UYS-1, two parallel registers are used (Figure 6). The SEC REG (Secondary Register, Figure 6) is used to build a 32-bit output word from the random number generator. After a 32-bit word is constructed, it is loaded into the OUTPUT REGISTER for transferring to Bulk Store. In this manner, the RNG is operated in a pipeline sequence to meet the speed requirement. Control for loading and reading the Main Register contents is done by the AN/UYS-1 programmer via the EDB/RTC interface board. The OUTPUT REGISTER strobe for putting data onto the ECDB is generated on the OSCBH Control Board.

D. DIGITAL-TO-ANALOG CONVERTER. Figure 7 is a block diagram of the D/A subunit. Each 32-bit Bulk Store word is first latched into the ECDB latch and then gets stored intc the D/A Memory. Depending on which half of the 64-bit double word was received, the 32-bit word is stored into either the lower half of memory (address space 0 - 31) or the upper half of the memory (address space 32 - 63). Therefore memory address bits 0 - 4 correspond to the channel number and bit 5 represents the upper or lower 32-bit word, i.e., channel 0 is equal to address 0 and address 32. After the memory is loaded with the required amount of data for updating the number of D/A channels, the D/A memory is cycled such that the samples are transferred to the Data Latches on the D/A boards. The latches are updated every Real Time Clock pulse.

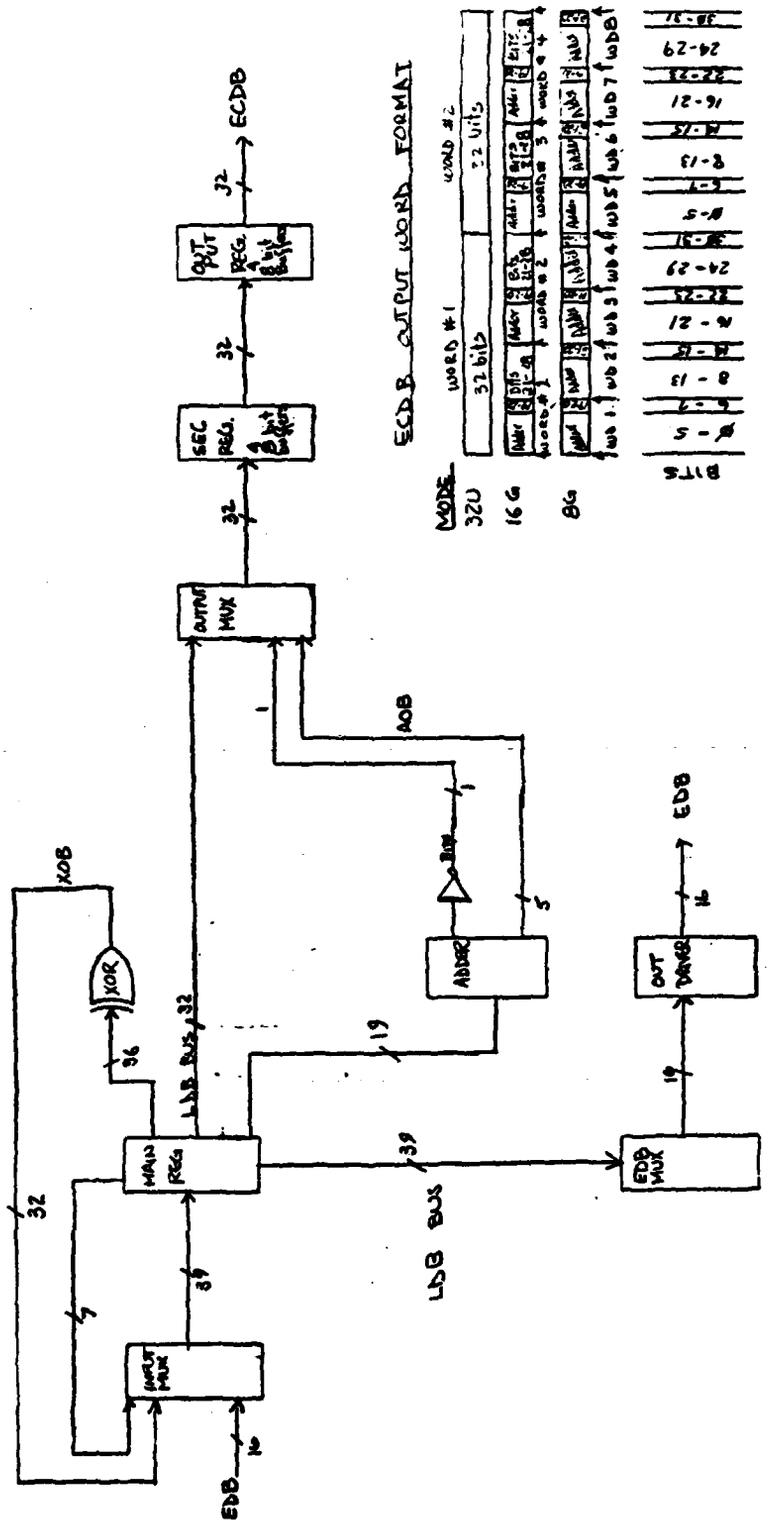


FIGURE 6 RANDOM NUMBER GENERATOR OVERALL FUNCTIONAL DIAGRAM

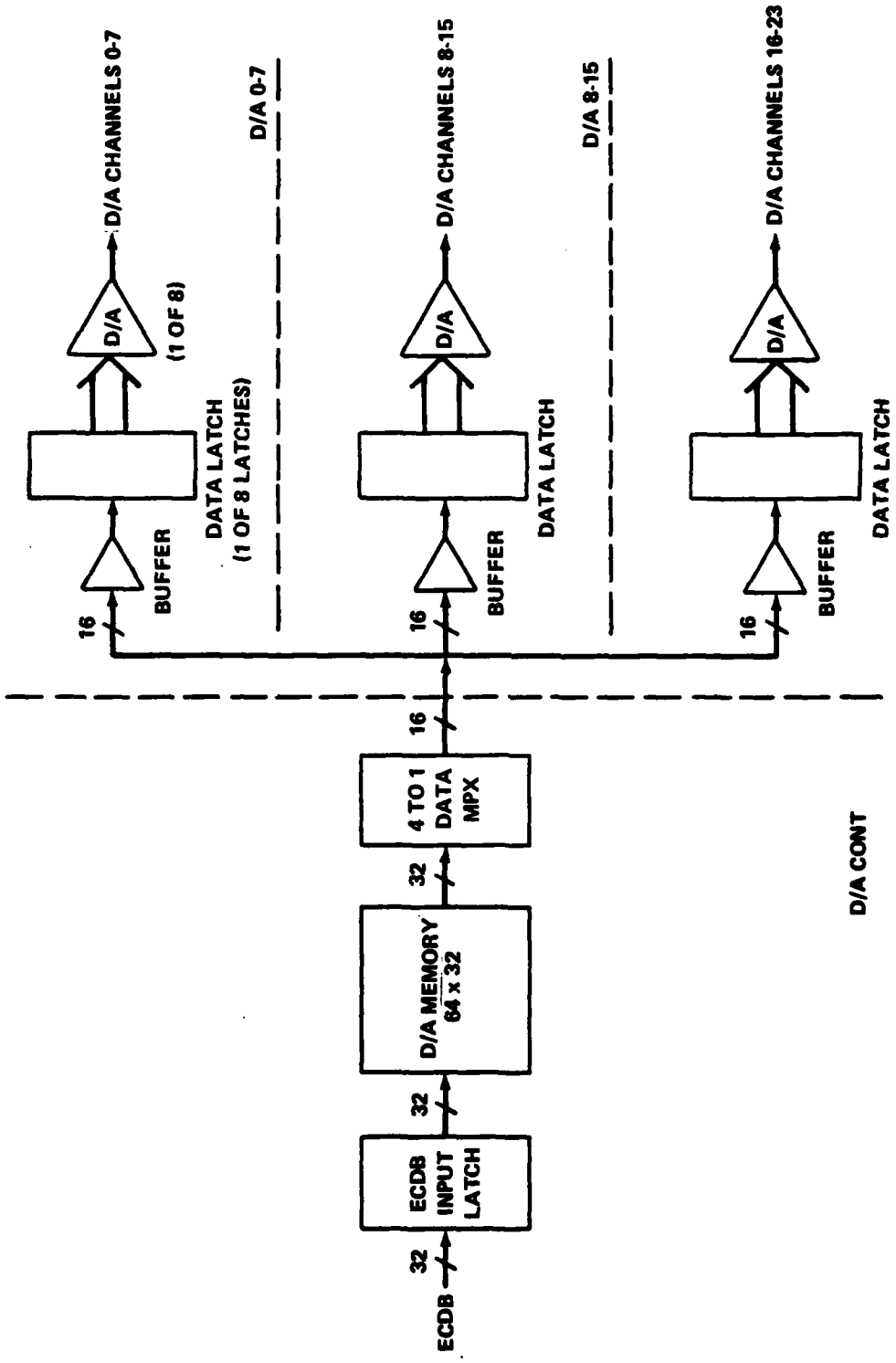


FIGURE 7 D/A BLOCK DIAGRAM

E. BASIC HARDWARE CONTROL. This section is required to generate the ECDB timing and control sequences necessary to transfer data to and from Bulk Store. The timing diagrams are shown[1] and reproduced in this report as Figure 8. Another function performed by this section is the generation of a series of initialization pulses to load the separate counters in the Bulk Store Address Generation logic at power up. The OSC BH status and mode registers are also located in this module. (Tables 2 and 3 show the bit assignments for these registers.) The remainder of the logic is concerned with the sequencing and control of the D/A and RNG subunits with the D/A section receiving a higher priority than the RNG.

[1]Ibid., pg. 11.

TABLE 1 EXTERNAL REGISTER ASSIGNMENTS

EXTERNAL REG/WORN	D/A High Order Initial Address	EDB OPERATION	BITS USED
78/0	D/A High Order Initial Address	WRITE	8-15
78/1	D/A Low Order Initial Address	WRITE	0-15
78/2	Number of D/A Buffers	WRITE	8-15
78/3	D/A Buffer Length per channel	WRITE	0-15
79/0	A/D High Order Initial Address	WRITE	8-15
79/1	A/D Low Order Initial Adress	WRITE	0-15
79/2	Number of A/D Buffers	WRITE	8-15
79/3	A/D Buffer Length per channel	WRITE	0-15
7A/0	RNG High Order Initial State	READ/WRITE	0-15
7A/1	RNG Mid Order Initial State	READ/WRITE	0-15
7A/2	RNG Low Order Initial State	READ/WRITE	0-6
7A/3	RNG High Order Initial Address	WRITE	8-15
7A/4	RNG Low Order Initial Address	WRITE	0-15
7A/5	RNG Buffer Length	WRITE	0-15
7B	DASS OSC STATUS	READ	0-15
7C/0	OSC MODE REGISTER	WRITE	0-15
7C/1	OSC RTC INTERVAL	WRITE	0-15

TABLE 2 OSC STATUS REGISTER

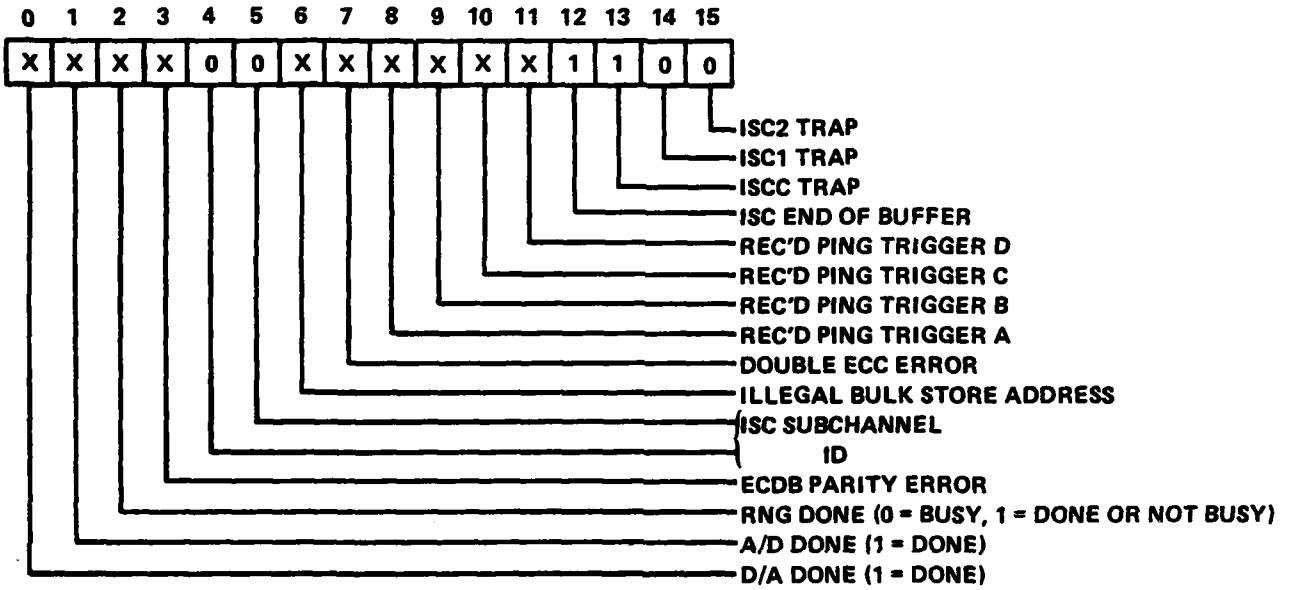
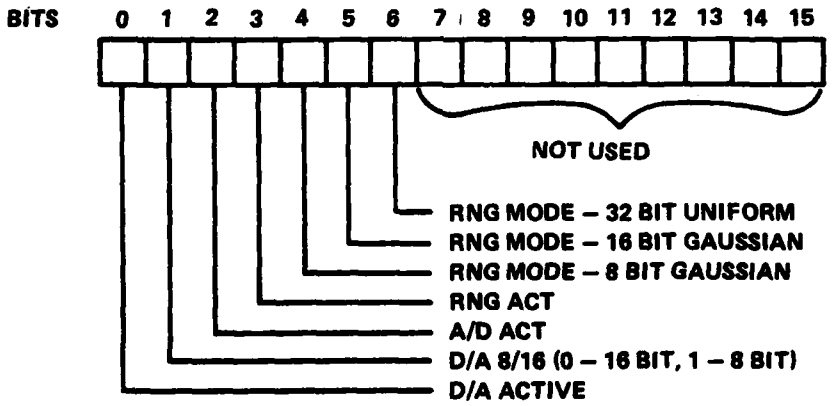


TABLE 3 OSC MODE REGISTER



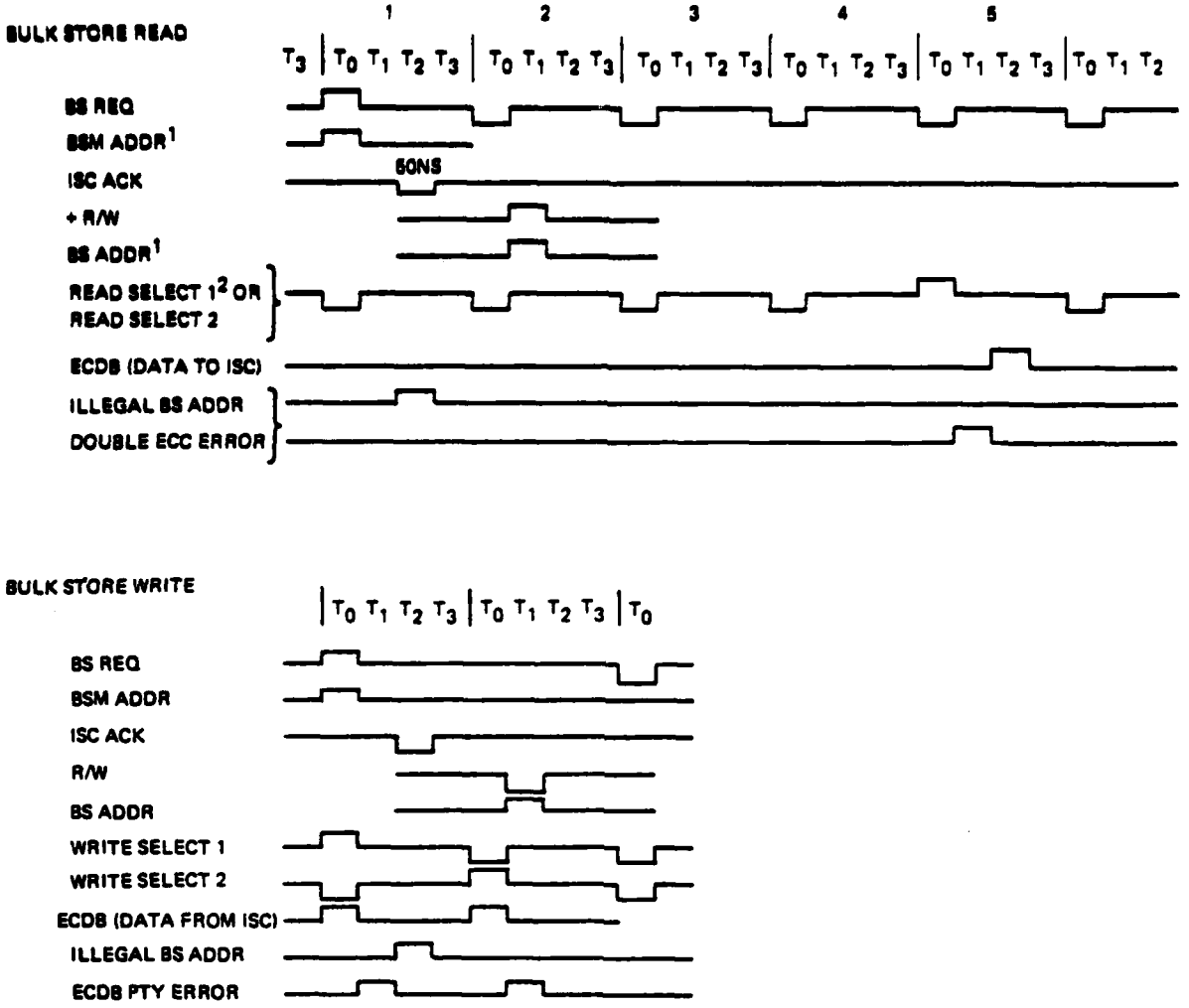


FIGURE 8 ISC TIMING REQUIREMENTS

CHAPTER 3

THEORY OF OPERATION

D/A OPERATION

The operation of the D/A section of the OSCBH is shown in the flowchart in Figure 9. This flowchart gives a functional sequence of the operation of the D/A converter. A detailed analysis will expand on this flowchart.

The initial process involves "setting up" the required parameters for the D/A control section. Table 1 shows the word assignments for the D/A parameters utilizing external register address 78. The circuitry that decodes the address and sends out the appropriate load pulse is on the EDB/RTC board. Figure A-12 shows the decoding circuitry and word counter, where C26* contains the write decoder and A33 and E33 the word counter logic. (The read and write operations are performed on the EDB bus in accordance with timing diagram, Figure 4.) This word counter is used to keep track of successive reads or writes to an external OSCBH register. The actual load signals are generated on Figure A-13 by NORing a count signal with the LDXR78 signal. The resultant signals are LDXR78/0 (first word, where the /0 signifies which word), LDXR78/1, LDXR78/2, and LDXR78/3. These signals are used to load the following registers respectively, D/A High-Order Initial Address (C41 on BSAG 1 board, Figure A-7), D/A Channel Counter (L42 and N42 on the BSAG2 board, Figure A-9) and D/A Buffer Length Register (G41 and E41 on BSAG2 board, Figure A-9).

The next step in the sequence is loading the mode register. The address is decoded via the same circuitry on the EDB/RTC board by J1-C (Figure A-13), strobing the data into the mode register located on the BSAGC board (at location R1 Figure A-6).

After the parameters and mode are stored, the RTC interval is loaded which also initiates the Real Time Clock. The RTC interval register load pulse is generated on the EDB/RTC board by J9-F (Figure A-13) and is labeled LDXR7C/1. This signal loads the interval register on the EDB/RTC board, locations L1 and L12 (Figure A-14), programming the four MC 4018 counters to generate the required RTC pulse period.

With the counters programmed, the first RTC pulse is used to initally transfer the D/A parameters from the storage registers to the active parts of the hardware, i.e., counters, address drivers, etc. This initialization

*C26 signifies the column (C) and location of pin 1 of the integrated circuit (IC 26) on an Augat^{R} circuit board. Also, if a letter follows, i.e., C26-A, this means the A section of an IC if it has more than 1 gate present per package.

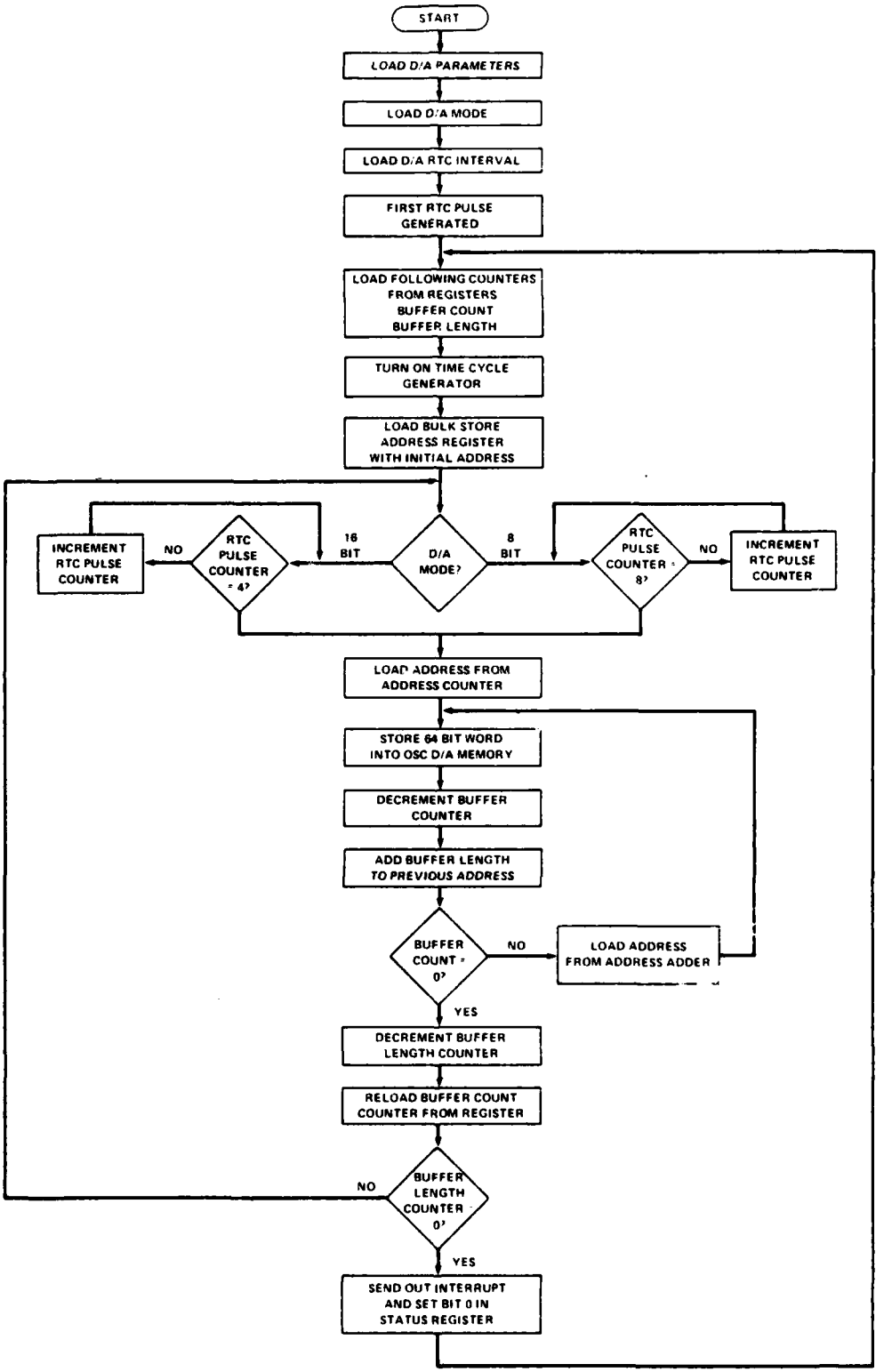


FIGURE 9 SEQUENTIAL OPERATION OF D/A LOGIC

circuitry is found on the BSAGC board (Figure A-1). The upper string of flip-flops (R36 and R28) and the serial to parallel register (V33) make up the initialization circuitry. When a RTC pulse arrives, it is first synchronized to the AN/UYS-1 T clocks generating a RTC SYNC, which sets the INIT 2 flip-flop (R28A, Figure A-1) causing the serial to parallel register to generate signals IP1 through IP5. In conjunction with the D/A operation, IP1 loads the D/A Address Counter on BSAG1 (Figure A-7) and the D/A Buffer Counter (channel counter) on BSAG2 (Figure A-9) and IP2 loads the D/A word counter on the BSAG2 card (Figure A-10). The last signal, IP5 is used to initiate the D/A control cycle on the BSAGC (Figure A-2) at C33-13, generating a GO signal. This sets the D/A ACT NOW flip-flop (C9-A on Figure A-4) (the D/A CYC flip-flop [A9-B, Figure A-4] was set high by the first RTC pulse). The IP5 signal triggers a START pulse on DWG A5 that sets the OSC ACT flip-flop (L17 DWG A5) and begins the data transfer operations for the D/A's.

With the TC Generator accivated (OSC ACT flip-flop set), the rest of the circuitry will realize the ECDB timing diagram of Figure 8. The BS REQ and BSM ADR OUT (signal that enables the BSM Address drivers) signals are generated by the START pulse. The two signals, BS REQ and BSM ADR OUT are sent out at TO. Because of the priority defined by the AN/UYS-1 hardware, the OSCBH (the OSCBH takes the place of an ISC unit) receives the highest priority in accessing Bulk Store over the ECDB bus, guaranteeing a maximum of three Bulk Store requests required for each initial access. To signify a successful access, ISC ACK is sent by the AN/UYS-1. This terminates the OSC Bulk Store requests and allows the TC generator to continue with successive time cycles, TC1, TC2, TC3, TC4, and TC5. During TC1, the ECDB R/W signal is sent to the AN/UYS-1 by driver C43-B on Figure A-2 along with the BS ADR OUT (to enable the Bulk Store Address drivers) generated by A44-D on Figure A-2. After a delay of two time cycles (800 nsecs) in which nothing is sent or received over the ECDB, a RD SEL 1 signal is generated by R12-8 flip-flop and sent by the driver J43-A during TC4 (Figure A-3). The requested data is then strobed into the D/A memory buffer (A9, C9, E9, and G9 on the D/A CONT card, Figure A-16) by the OSC DATA IN signal generated by G34 pin 6 on Figure A-2. This operation brings in the first 32 bits of data from Bulk Store. The second 32 bits of data are strobed in by activating RD SEL 2 (R12-B and J43-B on Figure A-3, BSAGC) during TC5 and using OSC DATA IN to strobe the data into the buffer on the D/A CONT card. This procedure constitutes the initial accessing of Bulk Store. If more than 1 channel of D/A data is requested by the user, the above operation is repeated until a D/A BC = 0 (D/A buffer count) is generated by L42-pin 13 (D/A Buffer Counter) on BSAG2, Figure A-9. This signal is then delayed by the circuitry on Figure A-5 (BSAGC) (C25-A, E44-A, C33-A, and V9-E, F) so that it occurs after the final 64-bit doubleword of data is received. The D/A Bulk Store address is taken from either the D/A address counters (A41, J43, L43, N43 and R43 on the BSAGL board, Figure A-7) or the BS Address Adder (T1, V1, T13, & V13) on the BSAG2 board (Figure A-8). Before continuing the Bulk Store Addressing circuitry description, a description of the D/A addressing and storage requirements will be reviewed.

The data for the D/A's are stored in Bulk Store as successive blocks of data with channel 0 starting at the first address, see Figure 2 and the rest of the channel blocks following. Referring to Figure 2, the OSCBH coordinates the transfer of a double word of data from the AN/UYS-1 to the D/A memeory. When it is determined that a new double word is required, the first address is generated

from the D/A Address Counter. This address would correspond to . base address. The next double word (corresponding to channel 1) is generated by adding the D/A buffer length to the value in the BS ADR REG (R5 and N5 on BSAG1, Figure A-11). After the first channel's data has been sent, the second and successive address generation is handled by the BS ADR ADDER (BSAG2 board, Figure A-8), BS ADR MPX (BSAG1 board, Figure A-11) and the BS ADR REG (BSAG1 board, Figure A-11), with each successive address resulting from the addition of the buffer length to the previous address. The BS ADR MPX (T19, T43, V19, V43, T7, T31, V7 and V31) is selected by HO MPX and LO MPX (both signals generated by G1 on BSAGC board, Figure A-4) to access the adder results after the initial access was made. This procedure is repeated until the buffer counter has decremented to zero.

The data transfer of the ECDB to the D/A Memory is accomplished on the D/A CONT board. Figure A-15 contains the ECDB INPUT BUFFERS (A9, C9, E9, and G9) and the D/A Data Memories (A20, D20, G20 and K20). Two strobe pulses are required per Bulk Store address in order to clock in a 64-bit double word off the 32-bit ECDB bus. Each strobe pulse has the dual role of strobing data first into the ECDB INPUT BUFFER and then into the D/A DATA MEMORY. The addressing of the D/A MEMORY is accomplished by the D/A OUTPUT COUNTER (A35 and C35 on Figure A-16) and DMA2 (Data Memory Address 2, Figure A-19) which are both generated on the D/A Control Board. The D/A Output Counter generates DMA (D/A Memory Address) bits 3-7, which defines the buffer count (corresponding to the D/A channel number) and DMA 2 (bit 2) which is used to identify either the first or second of a double word.

After the data has been loaded into the D/A DATA MEMORY, memory is read by the D/A's as either 8 or 16 bit bytes of data. This is accomplished by the DATA MULTIPLEXORS on the D/A Cont Card (N1, N10, R1, R10, T1, T10, V1, and V10, Figure A-16). The byte of data is selected by HO and LO DATA SEL which transfers a 16-bit word to the D/A boards. The correct 32-bit word is addressed by DMA-2 which is generated on Figure A-19 (G43 and J44). These signals then address a common byte in the D/A memory during each RTC period. The memory is then incremented via the DMA counter (A35 and C35 on Figure A-16) from D/A data words 0 through 31, with a corresponding load pulse being generated on Figure A-17 for strobing the data into the D/A buffers on the D/A cards. As the D/A memory is being cycled, the appropriate load pulse loads the data into a D/A buffer register to be converted by a D/A Converter. After all the data has been stored, D/A BC = 0 pulse is generated by L42 on the BSAG2, Figure A-9 and decrements the D/A WORD COUNTER (G1, G11, G21, G31 on BSAG2 board, Figure A-10). If the D/A WORD COUNTER does not go to zero, the D/A will repeat the data acquisition sequence (as shown in Figure 9, D/A flowchart). When the counter does count down to zero, a D/A WC = 0 pulse is issued by the D/A Word Counter on the BSAG2 board generating an interrupt for the AN/UYS-1 software and automatically reinitializing the D/A counters. The interrupt is sent to the AN/UYS-1 by G10 and R44 on the BSAGC card (A4). D/A WC = 0 sets bit 0 in the status word (flip flop N9-A on BSAGC, Figure A-6) indicating D/A done. The counters and buffers that get reloaded by this signal are the D/A BS ADR CTR (BSAG1, Figure A-7), D/A BUFFER LENGTH BUFFER (L1 and L13 on BSAG2, Figure A-9) and the D/A WORD COUNTER (G1, G11, G21, and G31 on BSAG2, Figure A-10).

*The D/A Buffer Counter is decremented at the very beginning of a D/A data cycle (T0 of TC0).

The D/A control then repeats the complete sequence using the new parameters to generate new D/A signals.

RNG SYSTEM DESCRIPTION.

The Random Number Generator (RNG) designed for the OSCBH is based on a previous design done at NSWC/WOL. This random number generator is based on a 39-bit shift register. Bits 38 and 34 of the shift register are Exclusive-ored and shifted into the MSB (bit 0) until a 16-bit uniformly distributed random number is generated. The Gaussian distributed numbers are then formed by adding bits 0-3 to bits 4-7 and bits 8-11 to bits 12-15 with bits 26 and 27 used as the carry in's into the adders respectively. These five bit sums are added together and bit 28 is used as the carry in. This six bit sum is used as the high order six bits of the Gaussian random number and bits 16-25 are used as the lower ten bits. This technique was found to provide an excellent means of generating random numbers and was selected for this application.

The OSCBH implementation of this design required a drastic increase in operating speed. To obtain the speed, the serially operated shift register needed to be modified. Figure 6 shows the architecture designed to implement the high speed random number generator. The shifting operation was performed by using a bank of Exclusive-or gates feeding back the transformed uniform 32-bit random number back to the main register. Thirty-six bits of the main register are exclusive-ored to give a 32-bit uniformly distributed number per clock pulse. The desired random number (which gets stored into the secondary register (SEC REG) is then formulated via the output multiplexor (OUTPUT MUX) to be either a 32-bit uniform, a 16-bit Gaussian distributed random number. From Figure 6 the summing logic described above for the previous design was implemented in a similar manner in this design.

Returning to Figure 6, the first step of the RNG operation entails loading the Main Register via the Input Multiplexor. This is performed by strobe pulses LDXR7A/0, LDXR7A/1, LDXR7A/2. Upon receipt of LDXR7A/3 (Table 1), the EDB bus is locked out and the serial register loop is implemented. The RNG sequence is initiated when the RNG is activiated by the BSAGC. The next operation is dependent on the RNG mode selected, a 32-bit uniformly distributed Random number, a 16-or 8-bit random number with a Gaussian distribution.

The 32-bit uniform mode only requires one 32-bit "shift" operation to be performed per 32-bit output word. After a shift operation the data in the Main Register is clocked into the Secondary Register during T1' (TX' defines a pulse that delayed 60 nsecs from the AN/UYS-1 TX signal and 40 nsecs wide and X is 0, 1, 2, or 3). This is the first half of the 64-bit word. At T2 the random number generator sequence is started for the second 32-bit word. To provide a place for the new word to go, the output register is loaded with the first 32-bit random number at T3. At the next T1', the second 32-bit word is loaded into the secondary register. The random number generator then waits for an ISC ACK to occur before a new 64-bit (two 32-bit words) double word sequence is initiated. After an ISC ACK is received from the AN/UYS-1, the second half of the word is loaded at T3 in order to be transmitted during the second half of the write cycle. In this way the Random Number Generator produces two 32-bit words at a time. See Figure 10 for timing details.

The 16-bit Gaussian mode requires two 32-bit "shift" operations per 32-bit word or four 32-bit shift operations per 64-bit double word. The sequence is initiated in a similar manner as above except that the adder is used to generate Gaussian data. After each shift a 16-bit word is loaded in the secondary register during T3 and T1' (see Figure 11). Then at T2 the sequence for the second 32-bit word (second half of 64-bit double word) is begun allowing the output register to be loaded at T3. At T3' the first half of the second word is loaded into the secondary register. After the secondary register is loaded, a new 64-bit sequence will not begin until an ISC ACK is received from the AN/UYS-1 in a similar manner as the previous operation.

The 8-bit gaussian mode requires four "shift" operations per 32-bit single word or 8 "shift" operations per 64-bit double word. The sequence is initially shifted a T2' with the first 8-bit byte clocked into Secondary Register at T3'. The next shift is at T3' and loaded into the Secondary Register and so on until the secondary buffer is full. At T3', (after the 8-bit word is loaded), the second half of the 64-bit double word sequence is begun. At T3 the output buffer is loaded from the secondary register. When T3' arrives (60 nsec after output buffer is loaded), the first 8-bit byte is clocked into the Secondary Register. When the Secondary Register is full and an ISC Acknowledge has been received from the AN/UYS-1 a new 64-bit double word generation sequence will begin (Figure 12).

All of these modes of operation require 450 nsec to generate the initial 32-bit Random Number from receipt of a Random Number Generator active command from the AN/UYS-1. This condition is accounted for by the operation of the control logic on the BSAGC board for generating the initial RNG block address.

An EDB Read Operation is implemented to allow the AN/UYS-1 to load the last 39-bit word used by the Random Number Generator into memory via the EDB bus. This operation can only occur when the Random Number Generator is off.

A method is utilized by the RNG to generate continuous blocks of random numbers. Whenever the RNG has been loaded via the EDB, the first operation is a shift operation. The output byte is generated from this initial shift. Continuing this process until the last word is generated, the main register contains a 39-bit word that has already been operated on. This is the 39-bit word read by the AN/UYS-1. Therefore, the AN/UYS-1 memory contains the last word used by the RNG. When the RNG is reloaded with this last word, the sequence will begin by first shifting the 39-bit word and then generating the random number. In this way, the random number generator will provide a continuous stream of data with no breaks between blocks.

RNG CONTROL LOGIC DESCRIPTION (RNG2)

All the descriptions that follow will require reference to the timing diagrams for the three RNG modes.

Figure A-25 contains the logic for using the main register. The four cycle flip flops are used to load the main register during the generation mode. The RNG is intially started when RNG ON is received from the BSAGC. This sets the init flip flop and transmits an init pulse at T2' (definition of this pulse is

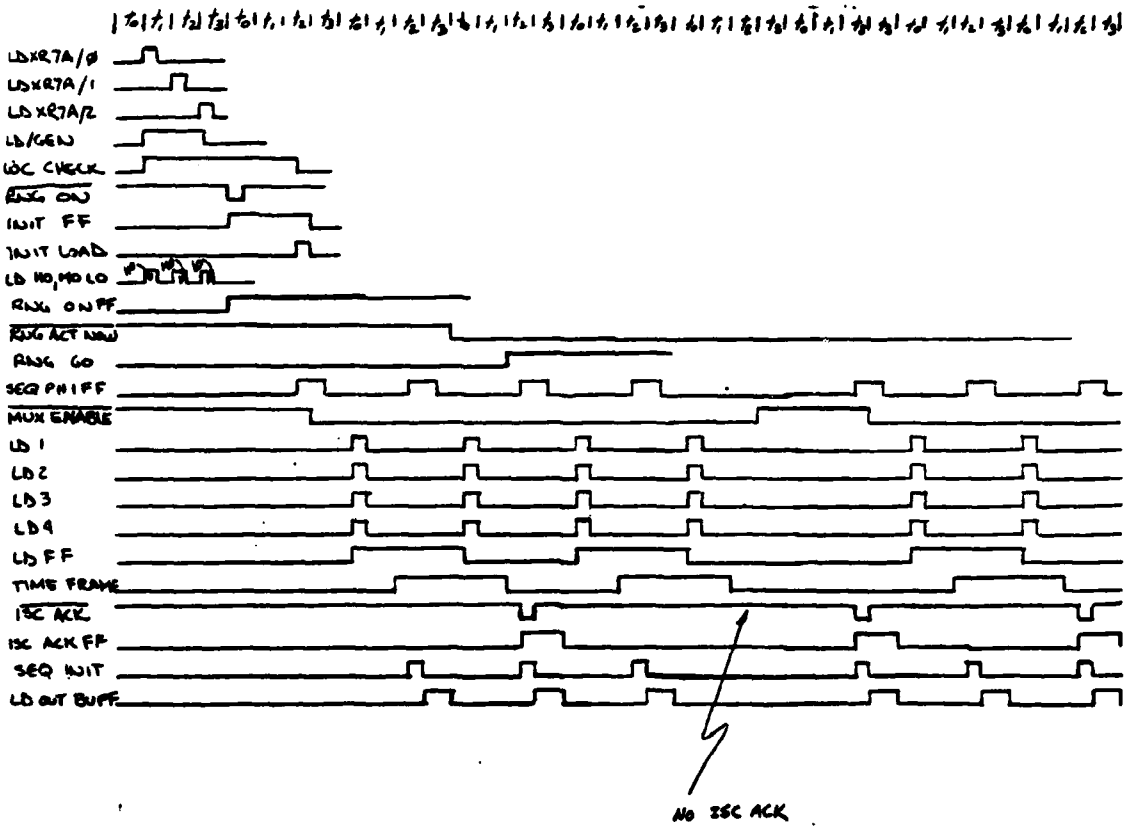


FIGURE 10 RNG TIMING – 32 BIT UNIFORM MODE D/A'S NOT ACTIVE

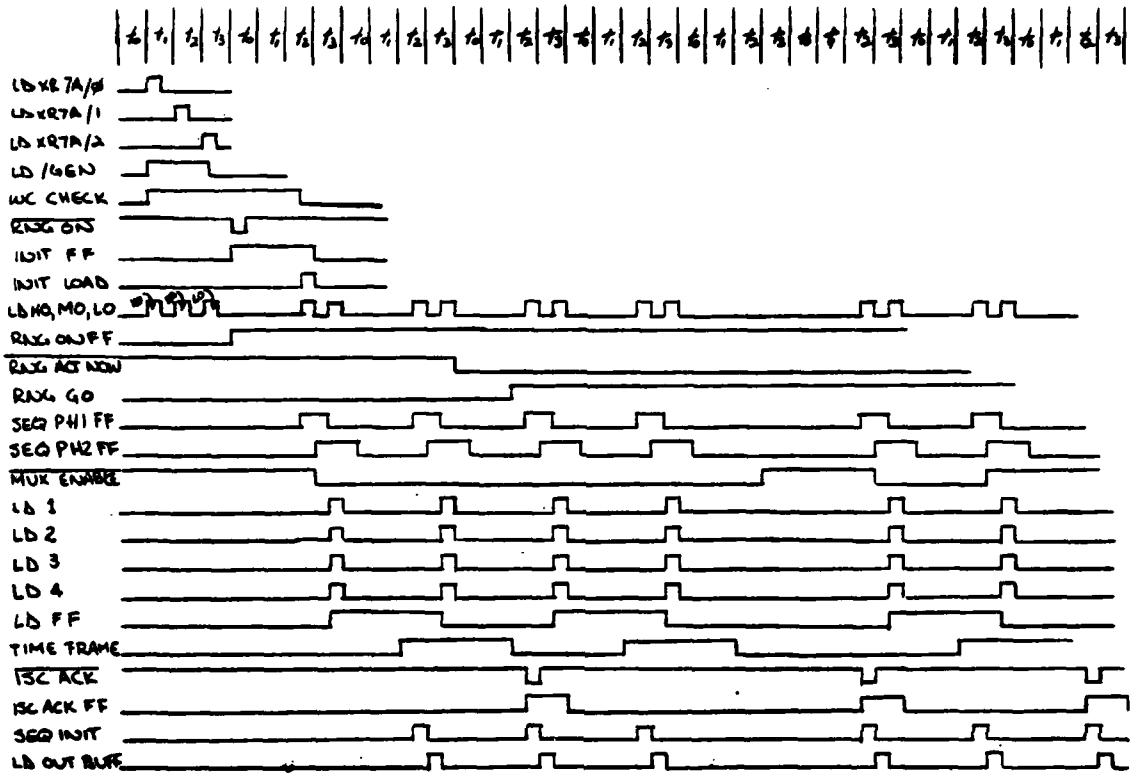


FIGURE 11 RNG TIMING – 16-BIT GAUSSIAN MODE D/A'S NOT ACTIVE

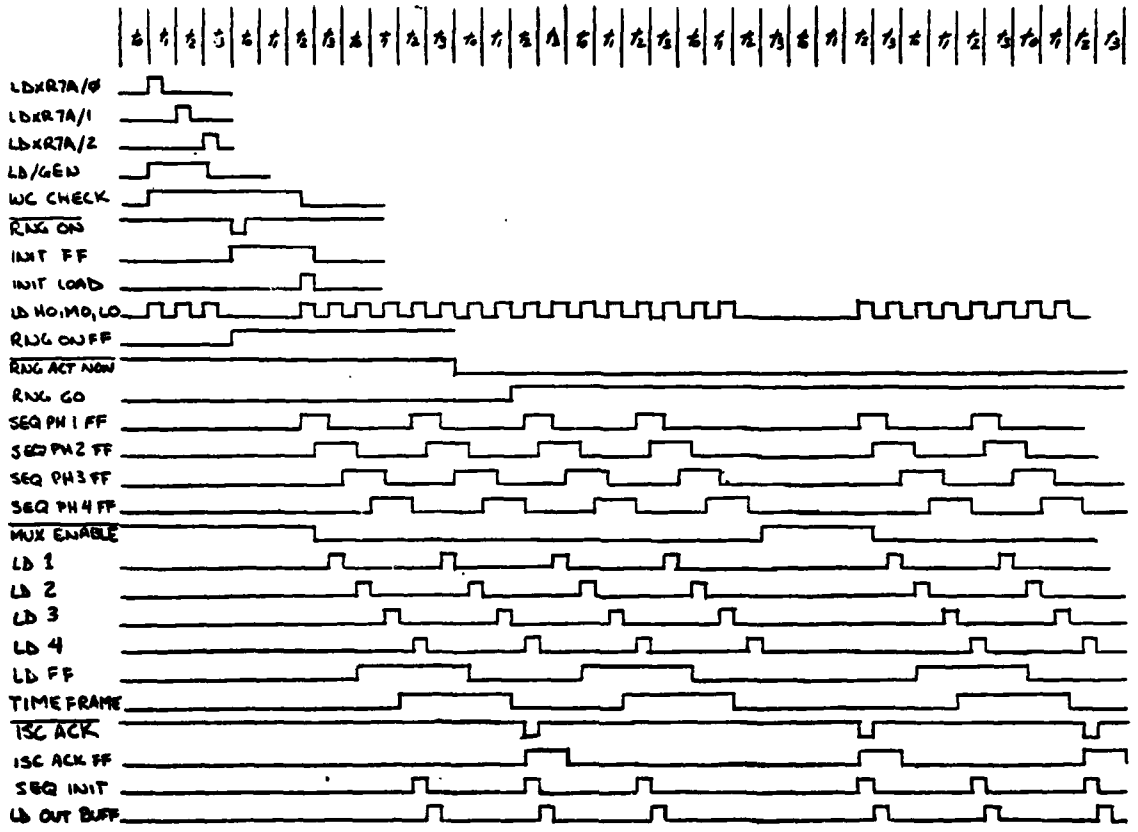


FIGURE 12 RNG TIMING – 8-BIT GAUSSIAN MODE D/A NOT ACTIVE

on Figure A-26). Then, when the RNG is active, it "shifts" the main register by reloading it from the bank of Exclusive-or gates. Continuing the cycle sequence to cycles 2, 3, and 4 depends on the mode selected. The LD, HO, LD MO, and LD LO signals provide strobes for the segmented main register.

Figure A-26 has the pulse generators for T0', T1', T2', and T3', and control flip flops. The T clocks are generated 60 nsec after the AN/UYS-1 T clocks with a 40 nsec duration. These clocks are used in conjunction with the AN/UYS-1 clocks to provide sequential operation of first loading the main register and then the secondary register. Therefore, whenever a T' clock is discussed it stands for a pulse generated 60 nsec after the designated T clock and 40 nsecs wide. The three flip-flops have various operations. The RNG GO flip flops, synchronizes RNG ACT NOW (generated by LDXR7C/0 with RNG set) to T2. This is used to synchronize the operation of the RNG to the address generation logic on BSAGC. After this signal goes high, 600 nsecs of time is available to generate the first 32-bit random number. The EDB OUT signal is used to signal the output drivers that the RNG is off and the 39-bit data word can be sent out over the EDB to the AN/UYS-1. The LD/GEN FF indicates the span of time from LDXR7A/0 to LDXR7A/2 for loading the main Reg. The RNG ON FF is used to turn the RNG control logic ON. This flip-flop gets reset when the word counter is zero.

Figure A-27details the output buffer and the secondary register load logic. The output register load logic in the left hand corner produces two signals, SEQ INIT and LD OUT BUFF. The SEQ INIT signal is generated during T2' (whenever LD 4 occurs within the window of T2) and is used to initiate another Random Number sequence. At T3, LD OUT BUFF is generated to transfer the data from secondary register into the output register.

The ISC ACK flip flop is used to signify that the first 32-bit word has been successfully written to the ASP and the second 32 bit can be loaded into the output register for transfer. The secondary register load controller is used to load the secondary register in the correct sequence (depending on the mode) whenever the MUX ENABLE signal is low. The SEC TIME FF is set by sampling the CYCLE 1 FF at T3 to determine if there is an active cycle. Figure A-28 is the schematic of the secondary and output registers used. As can be seen, the secondary register is divided into four, 8-bit bytes to be loaded individual or at once (depending on the mode). The WC CHECK FF is used to indicate a continuation situation in the RNG and therefore transfer whatever is in the output register for the first word.

The timing diagrams for 8-bit Gaussian, 16-bit Gaussian and 32-bit uniform random number modes are shown in Figures 10, 11, and 12.

RNG - AN/UYS-1 INTERFACE

This section describes the operation of the RNG (Random Number Generator) and the OSCBH interface control circuitry. On the Output Signal Conditioner Block Diagram (Figure 3), the RNG encompasses two cards in the rack. The RNG-AN/UYS-1 interface logic is used to interface the RNG with the AN/UYS-1. To help visualize the system operation, a flowchart of the sequence for generating a random number is shown in Figure 13. The following description describes the RNG-AN/UYS-1 interface logic.

The initial step in the sequence is loading the RNG parameters (given in Table 1) into the OSCBH. The first three words transferred comprise the initial state of the RNG and are loaded into the MAIN REGISTER. The next two words make up the initial BS address and are stored on BSAG2 card (A9, V31, and V41). As with the D/A section, the load pulses for these latches are generated on the EDB/RTC card. This procedure entails decoding the address on the EAB (External Address Bus) and keeping track of the successive accesses. The decoding of the address is performed by C26 on Figure A-12 and the word count is generated by A33 Figure A-12. The final load signals are generated by NORing LDXR7A (C26 signal) with WC = 0 through WC = 7 (generated by A33 and E33). The NOR gates are located on the EDB/RTC card (Figure A-12, IC's J9 and J1) and are labeled LDXR7A/Y where Y denotes the word counter value.

The first signal generated, LDXR7A/0, sets a flip flop on RNG Control Card (A26, E10) called LD/GEN. This signal is used to load the main register with the initial state (from the EDB bus). LD/GEN generates LDHO on RNG2 (A25) which loads the High Order 16 bits of the state into the High Order Section of the Main Register(V19, V20, V21). LDXR7A/1 generates LDMO on RNG2 (A25) and loads the middle 16 bits of the state into the second part of the Main Register (V15, V16, V17 on A20). Finally LDXR7A/2 generates LDLO on RNG2 (A25) and loads the final 7 bits of the state. The next two load pulses, LDXR7A/3 and LDXR7A/4 load the RNG Initial Address and gets stored on BSAG1 (Figure A-7 IC's C17, E17, and G17). This address is transferred to the RNG BS Address counter (Figure A-8 and A17, J19, L19, N19, R19) on the falling edge of LDXR7A/4. The final parameter, buffer length, is stored into V31 and V41 (Figure A-9, BSAG2).

After the parameters have been loaded, the mode register (XR7C) is loaded with the type of random numbers desired (32-bit uniform, 16-bit Gaussian or 8-bit Gaussian) and RNG ACTIVE bit set. The RNG Active signal is set at the RNG ACT flip flop, E1-A (RNG ACT) on Figure A-4, BSAGC, to a 1 (and RNG ACT to 0), signifying that the RNG is busy. RNG ACT is brought out to the user as bit 2 in the status word. Upon loading XR7C another pulse is generated, RNGON (A25-8, Figure A-4). Because of the set up time requirement for the RNG, a time delay is required to set up the first two RNG words in the pipeline. RNG ON pulse is used to turn on the TC generator via the START SYNC and START flip flops on Figure A-2. The time delay is obtained when the RNGON flip flop is clocked at TC1. The delay achieved would then be at the least 600 nanoseconds which is used to preset E1-6 (RNG ACT NOW flip flop on Figure A-4). The activation of the RNG ACT NOW flip flop initiates the control sequence for sending data to Bulk Store.

The first in the control sequence for transferring data to Bulk Store is the activation of the TC generator (L25 on Figure A-2, BSAGC). This generator creates the time cycles involved in realizing the interface requirements of Figure 8. The TC generator is started via the RNGON pulse as described above. The initial Bulk Store address is loaded by the First Access flip flop, E33-B, on Figure A-5 (BSAGC). This flip-flop is set by RNG ACT NOW causing the address to be loaded 400 nsecs before it is needed which allows the address to be read at the beginning of the next write cycle. The BS REQ signal is generated by N17 (BS REQ FF, Figure A-2 on BSAGC) and driven to the ASP with C43A on Figure A-2. The BSM (Bulk Store Module) address driver (address drivers reside on BSAG1, Figure A-11, A1 & C1) enable pulse is generated by A44-D (BS ADR OUT) on BSAGC,

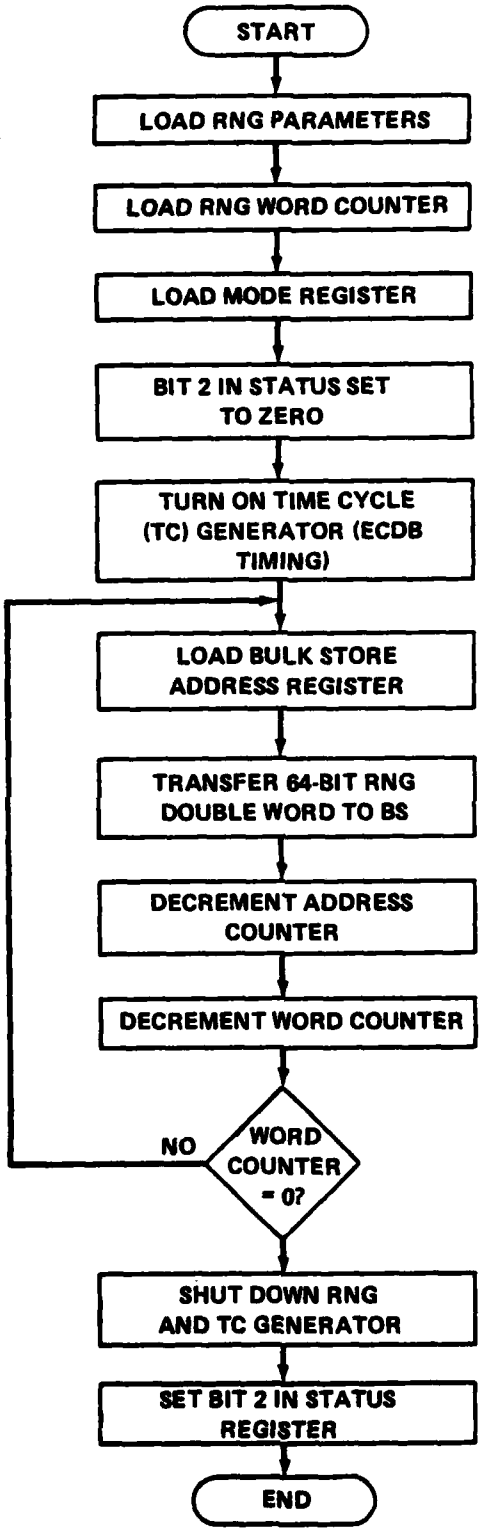


FIGURE 13 RNG CONTROL LOGIC

Figure A-2. The ECDB R/W driver is enabled by N33-F (ECDB R/W OUT) on BSAGC, Figure A-2. The WRT SEL 1 and WRT SEL 2 lines are set and coordinated by T12-A, T12-B, J43-B on Figure A-3 on BSAGC. Finally, the ECDB data drivers (located on RNG2) are enabled with OSC DATA OUT, V17-12 on Figure A-3 (BSAGC). These control signals described are used to send data and control signals to the AN/UYS-1.

The signals sent to the OSCBH are ISC ACK, ILLEGAL BS ADDR, ECDB PTY ERROR and double ECC ERROR. The first signal, ISC ACK, is used by the OSCBH to generate CC2 (Clear Control 2, on BSAGC, Figure A-2). CC2 resets the BS CYC REQ and BS REQ flip flops (N17-A and N17-B on Figure A-2) signifying that a successful access has been made. Then by resetting and setting the BS CYC REQ flip, a write cycle would be defined. The reason for the TC generator's dependence on BS CYC REQ is the possibility of conflicts within the AN/UYS-1 in which case the first OSC BS REQ may not be recognized. If an ISC ACK is not received by N17-A (BS CYC REQ flip flop, Figure A-2), TC0 is stretched resulting in retransmission of the BS REQ and BS Address until one is received. Upon receipt of an ISC ACK the TC generator continues to TC1 completing the write operation.

The actual control operation of the OSCBH during a write operation encompasses the coordination of the parameter counters. The RNG BS ADR COUNTER on BSAG1 (Figure A-8, J19, L19, N19, and R19) is decremented by DEC RNG WD CTR (generated at G10-6 on BSAGC Figure A-4). The RNG WORD COUNTER on BSAG2 (Figure A-10, E1, E11, E21, E31) is also decremented with DEC RNG WD CTR with RNG WC = 0 being generated when the count goes to zero (BSAG2 Figure A-10). This signal signifies that the block has been completed and the RNG is to be shut down. To allow the last cycle to complete, RNG WC = 0 is delayed on BSAGC (Figure A-5, E25) to occur 700 nanoseconds into the final WRITE CYCLE. This signal, RNG WC = 0 DEL, shuts down OSC ACT flip flop (L17) and the TC GEN (L25) on BSAGC, Figure A-2 and also resets RNG ACT NOW flip flop (E1) and RNG ACT (E1) on BSAGC, Figure A-4. By resetting RNG ACT, bit 2 in the status word (7B external register) is set, signifying that the RNG is "NOT BUSY".

This would complete the tranmission of a block of data to the AN/UYS-1.

RNG-D/A CONFLICT DESCRIPTION

The discussion up to now has described the operation of the Output Signal Conditioner with only one mode active at any one time (i.e., D/A's active or Random Number Generator active), but unfortunately this is not always the case. When the system is used in a real time simulation situation, the D/A's will be running continuously, providing analog signals for external use, and the RNG would be used on demand to generate blocks of data for the simulation computation. There are two conditions of conflict: a. The D/A section is accessing memory (D/A ACT NOW is high) and the RNG needs to be activated (load XR7C (mode) with RNG ACT bit set) and b. the RNG is active and the D/A section has to access memory to get new data from Bulk Store. Due to the requirement that the D/A output should be continuous, the D/A section has priority over the RNG. This entails for case (a) that the RNG would be started after the D/A section has finished and for case (b) that the RNG would be shut down long enough for the D/A section to finish it's data transfer and then be restarted.

The control circuitry that coordinates these two cases is located on BSAGC. For case (a), the condition of the OSCBH before the RNG activation signal is received is represented by the D/A ACT NOW flip-flop (C9-A on FigureA-4) being set and ACT CYC is high (A25-6 on Figure A-4) or ACTCYC is low (A17-4 on Figure A-4). When a LDXR7C/0 (load mode register) is received with Bit 3 of the mode word set (RNG ACTIVE bit), the RNG ACT flip flop (E1-A on Figure A-4) is set. The RNG ACT NOW flip flop (E1-B on Figure A-4) is used to indicate the status of the RNG request of the RNG request in the OSCBH. From the previous description of the RNG-AN/UYS-1 control logic without the D/A section being active, RNG ACT NOW would be set (activating the RNG). To resolve the conflict of case (a), the RNG ACT status bit would be used to turn on RNG ACT NOW whenever the D/A section gets done, (E1-B (RNG ACT NOW flip flop on A-4)uses RNG ACT for the D input). The strobe signal used to signify the end of a D/A access cycle is D/A BC = 0 (D/A buffer count (number of channels) = 0), which ripples through E17-B, J17-C, and finally G18-8 (Figure A-4) to clock the input of the RNG ACT NOW flip flop. In this way, the RNG is activated after the D/A has finished its cycle.

For case (b), an orderly shutdown of the RNG is needed before the D/A section is activated. To realize this condition the generation of an RNG HALT signal at each RTC pulse was implemented. This pulse would first shut the RNG down and then ripple through the ACT NOW flip flops (D/A and RNG) to determine if the D/A needs servicing. In this way, if the D/A's needed servicing, the RNG HALT is used to set D/A ACT NOW flip flop (C9-A). If the D/A's don't require servicing, the RNG ACT NOW signal would be set 40-60 nsecs after the HALT pulse was issued. Because of the short delay caused by the RNG HALT signal relative to the logic on the RNG control load, the RNG would continue generating random numbers as if there was no interruption. To guarantee no RNG dropouts, the RNG HALT pulse is generated at the end of a 64-bit random number WRITE CYCLE. The operation of the RNG HALT pulse is used to restart the TC generator and its associated circuitry by setting G44 (START SYNC and START flip flops) on Figure A-2(the RNG HALT pulse is transformed into TRANSITION HALT by E44-D on Figure A-2) thereby starting the OSCBH in a completely new cycle when the D/A converters need servicing. The timing diagram shown in Figure 14 shows the effect of the shut down procedure generated by the OSCBH control board on the RNG control logic.

In this way the two functions of the OSC conflicts are resolved without sacrificing a great deal of speed in the RNG.

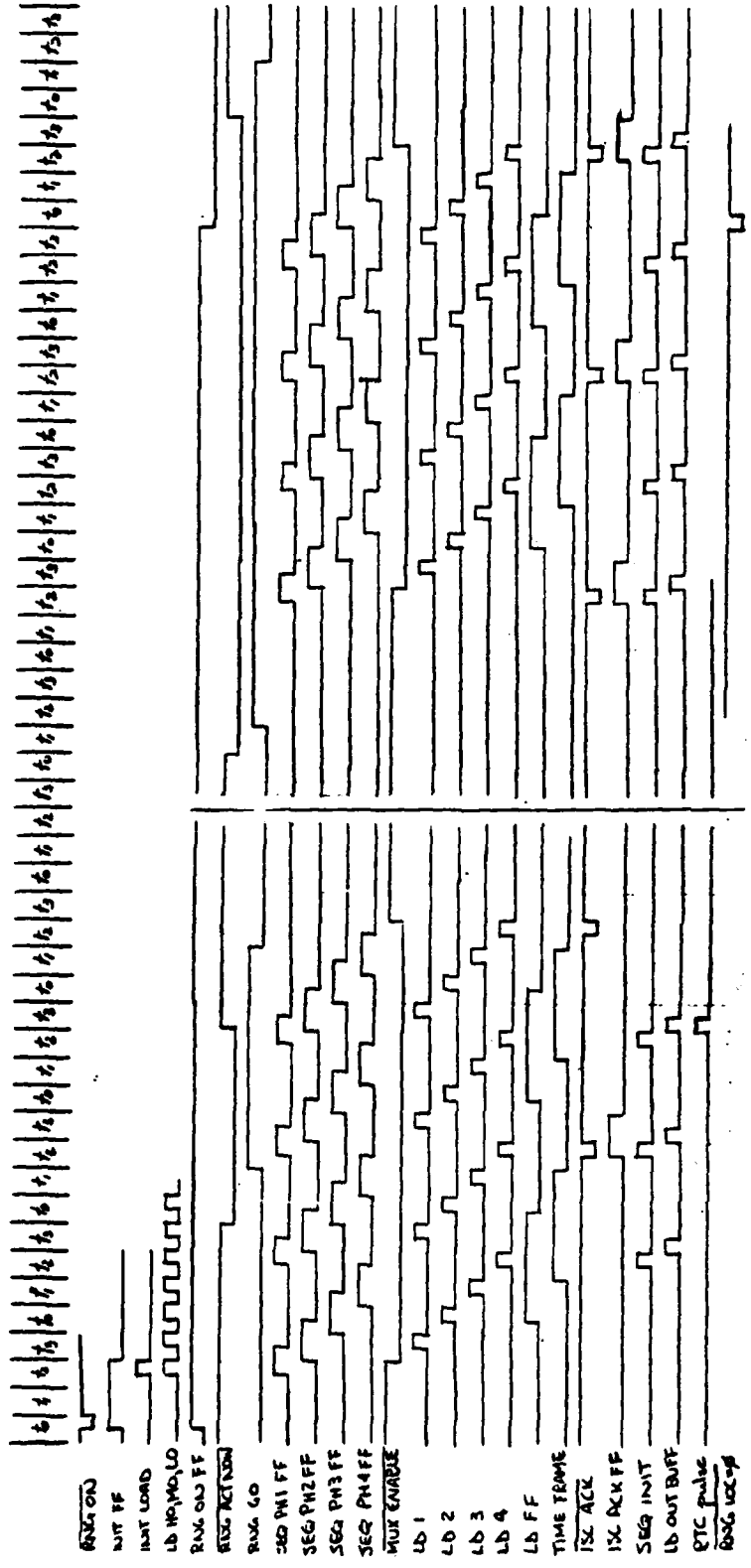


FIGURE 14 RNG TIMING (8-BIT GAUSSIAN MODE) D/A'S ACTIVE

CHAPTER 4

CONSTRUCTION AND PACKAGING

The OSCBH was constructed and packaged with standard wire-wrap techniques and components. This method was taken to ease development time and cost. Standard Augat^R components were chosen for the racks, backpanel, and circuit cards. To limit cabling problems and complexity, ribbon cable was chosen to interface the signals between the AN/UYS-1 and the OSCBH.

The two main busses that were extended to the OSCBH were the Error Corrected Data Bus (ECDB) and the External Data Bus (EDB) from the AN/UYS-1 Input Signal Conditioner (ISC) main-frame connectors. The length of the ribbon cabling was chosen to be five feet. Appendix B contains the wire lists of the ribbon cable connection. The signals were arranged so that at least one ground wire separated every signal line. The cable was terminated at the Augat^R rack backplane with ribbon cable dip sockets. Upon termination, the ribbon cable sockets translates the grounds and signals onto opposite lines. This method was selected because the Augat^R backplane was found to provide a handy means of grounding one row of the socket. If you look at an Augat^R backplane, it is constructed such that you have an empty connector slot between each connector position. This is done to accomodate the double width Augat^R boards (the Augat^R pins require the extra width). To ground the cable socket, a metal "comb" is inserted into the corresponding empty slot column and then grounded. In this way, when the socket is inserted onto the backplane, all the grounds between the signals are grounded. Figure 15 shows the backplane socket layout.

The wiring lists for the backplane circuitry are contained in Appendixes B and C. The pin assignments for each Augat^R card are contained in Appendix D.

Finally, the connector layouts for the Output Signal Conditioner Basic Hardware enclosure are shown in Figure 16.

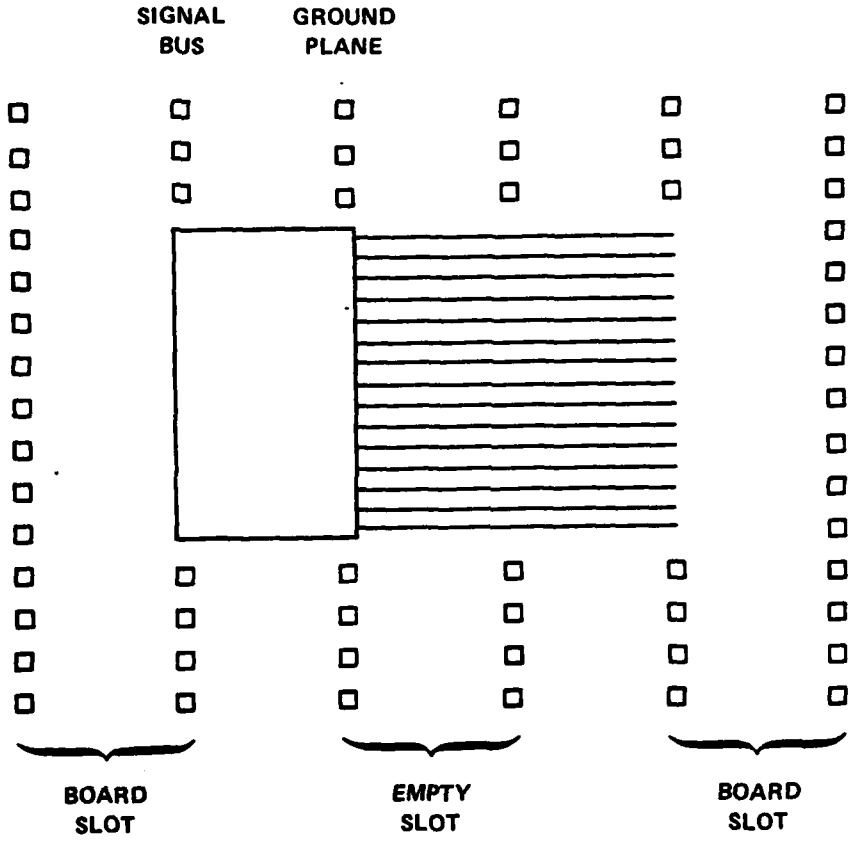


FIGURE 15 AUGET GROUNDING SCHEME

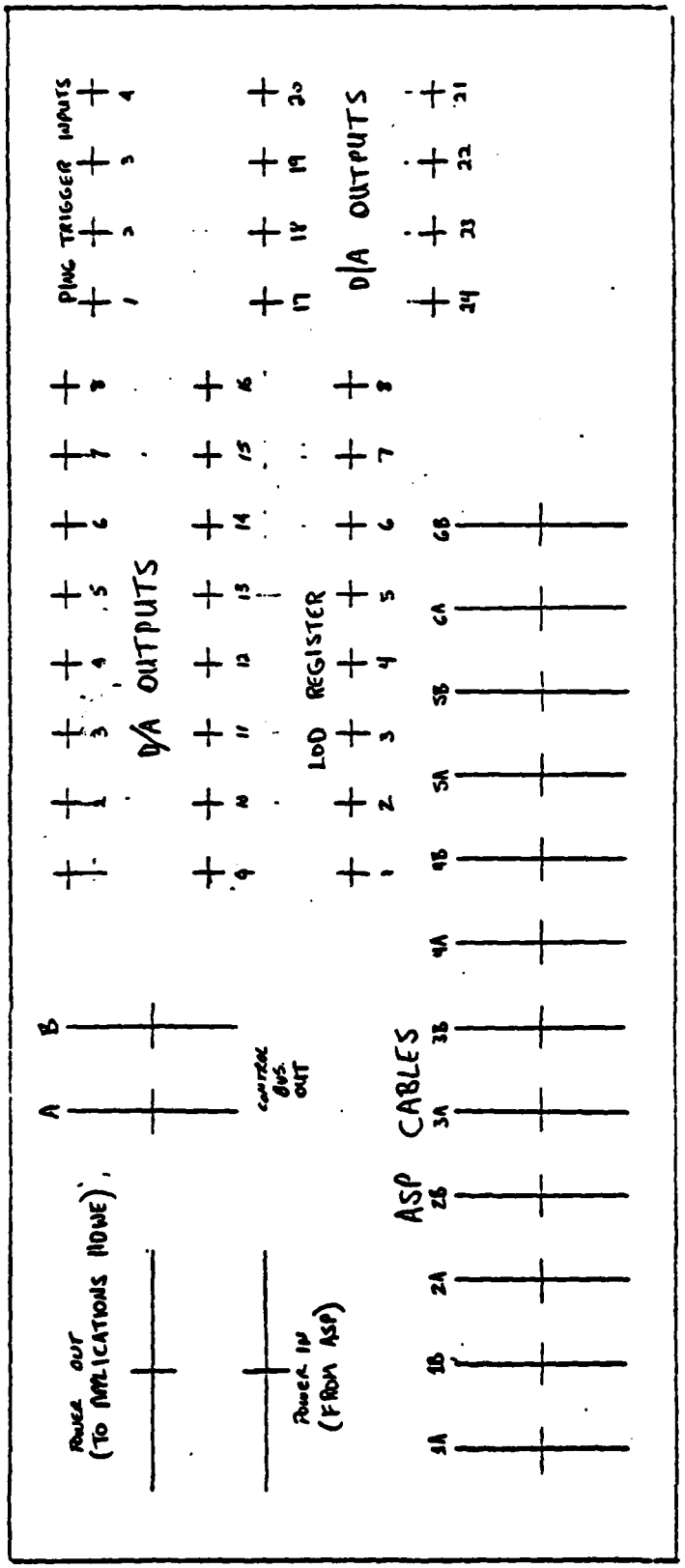


FIGURE 16 BASIC HARDWARE I/O

CHAPTER 5

DIAGNOSTIC SOFTWARE

BASIC HARDWARE DIAGNOSTICS

This set of diagnostics is used to check the Basic Hardware circuitry, specifically the RNG and D/A subsections. The diagnostic program has four basic objectives, to test the RNG and D/A sections alone, to test conflicts within the OSCBH when the RNG and D/A's are both enabled, to test OSCBH interference with AN/UYS-1 operation and finally to test AN/UYS-1 interference with OSCBH operation. Figure 17 is a flowchart of the Basic Hardware diagnostics. Figure 18 is a flowchart of RNGTES which is used by the Basic Hardware diagnostics to exercise and test the Random Number Generator. A detailed description of the program follows.

From Figure 17, the first two statements transfer a new Program Status Word (PSW) into the New Machine Check PSW location, $6A_H$, allowing any machine check errors to jump to the interrupt routine in the diagnostic software. The next operation checked is the EDB transfers. These transfers provide the OSCBH with parameters and commands and the AN/UYS-1 program with OSCBH status and RNG condition. The test entails first enabling the Machine Check interrupt hardware in the AN/UYS-1 and then performing some transfers to the OSCBH. If there are any irregularities detected on the EDB, a Machine Check interrupt would be issued. Three types of EDB errors are detected as a Machine Check:

1. EDB timeout
2. EDB parity error WRITE
3. EDB parity error READ

Upon detection of a Machine Check interrupt, the program jumps to a DIAG 0,0,0 instruction which effectively stops the processor and allows the condition of the AN/UYS-1 to be accessed using the maintenance panel. The OSCBH operations performed are setting the OSCBH mode to 0 (Write operation), reading the OSCBH status and reading the RNG seed. After these operations are performed the Random Number Generator is tested. For this, the machine Check interrupt is still enabled but a new Input Signal Conditioner (ISC) New PSW is loaded into location $7C_H$ to allow the AN/UYS-1 to field OSCBH interrupts.

The first test checks to see if the correct seed is loaded into the RNG. This is performed very simply by writing a seed into the RNG and reading it out again before the RNG is started. A comparison is then made on what was sent to what was read from the RNG, stopping execution whenever the two do not match. This test checks the EDB receivers and drivers in OSCBH. The External Address

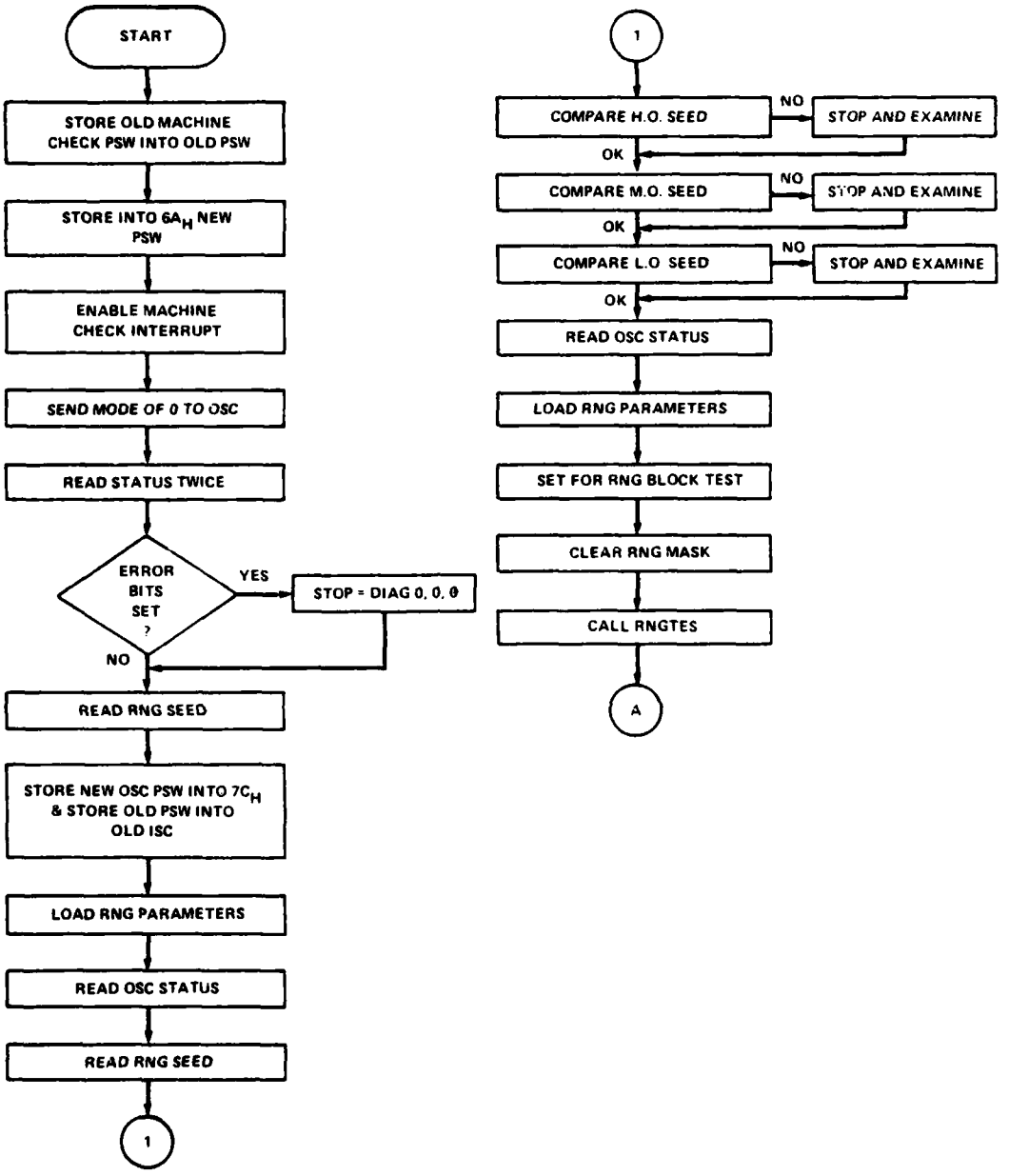


FIGURE 17 BASIC HARDWARE DIAGNOSTICS (1 OF 3)

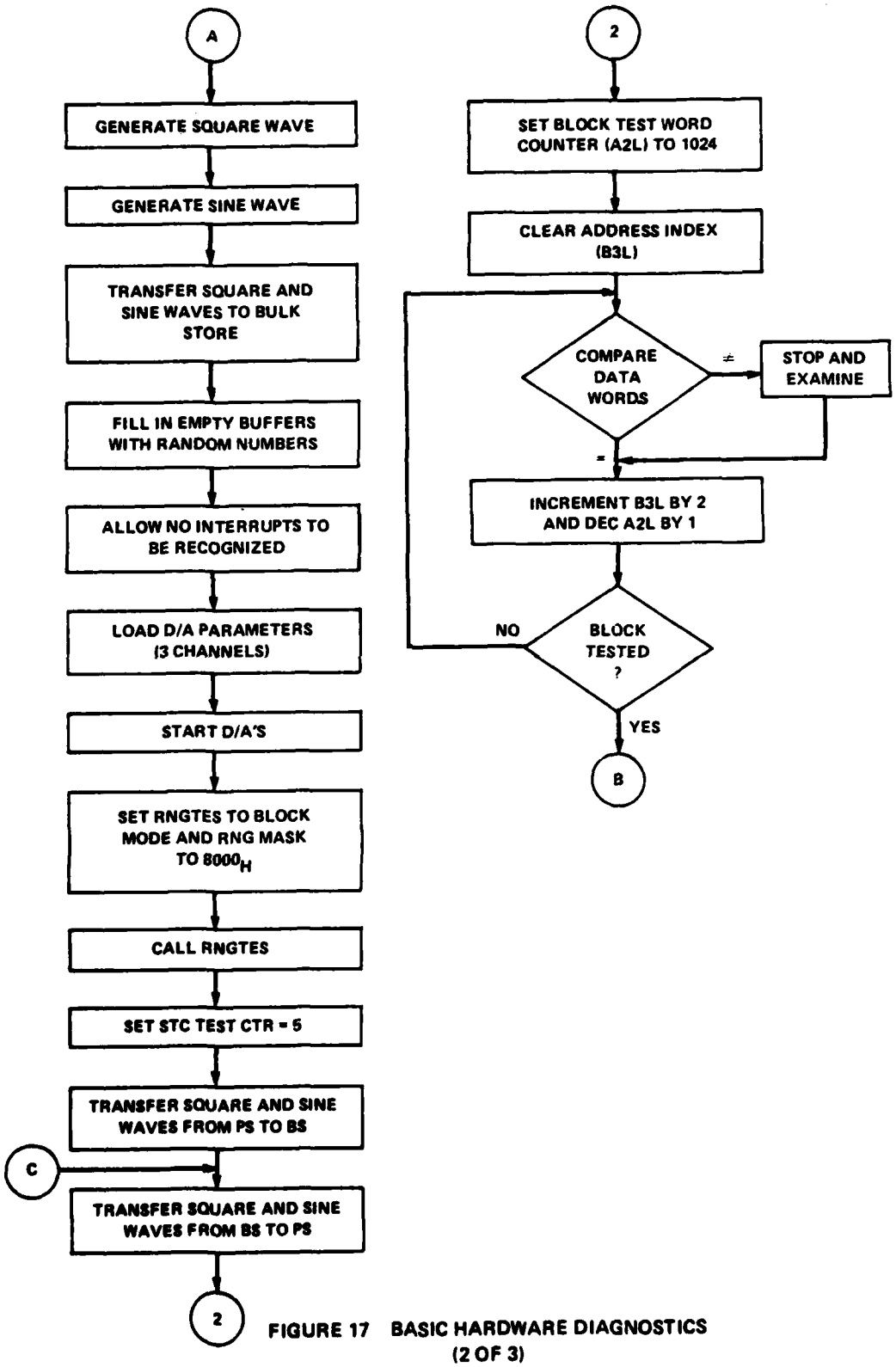


FIGURE 17 BASIC HARDWARE DIAGNOSTICS (2 OF 3)

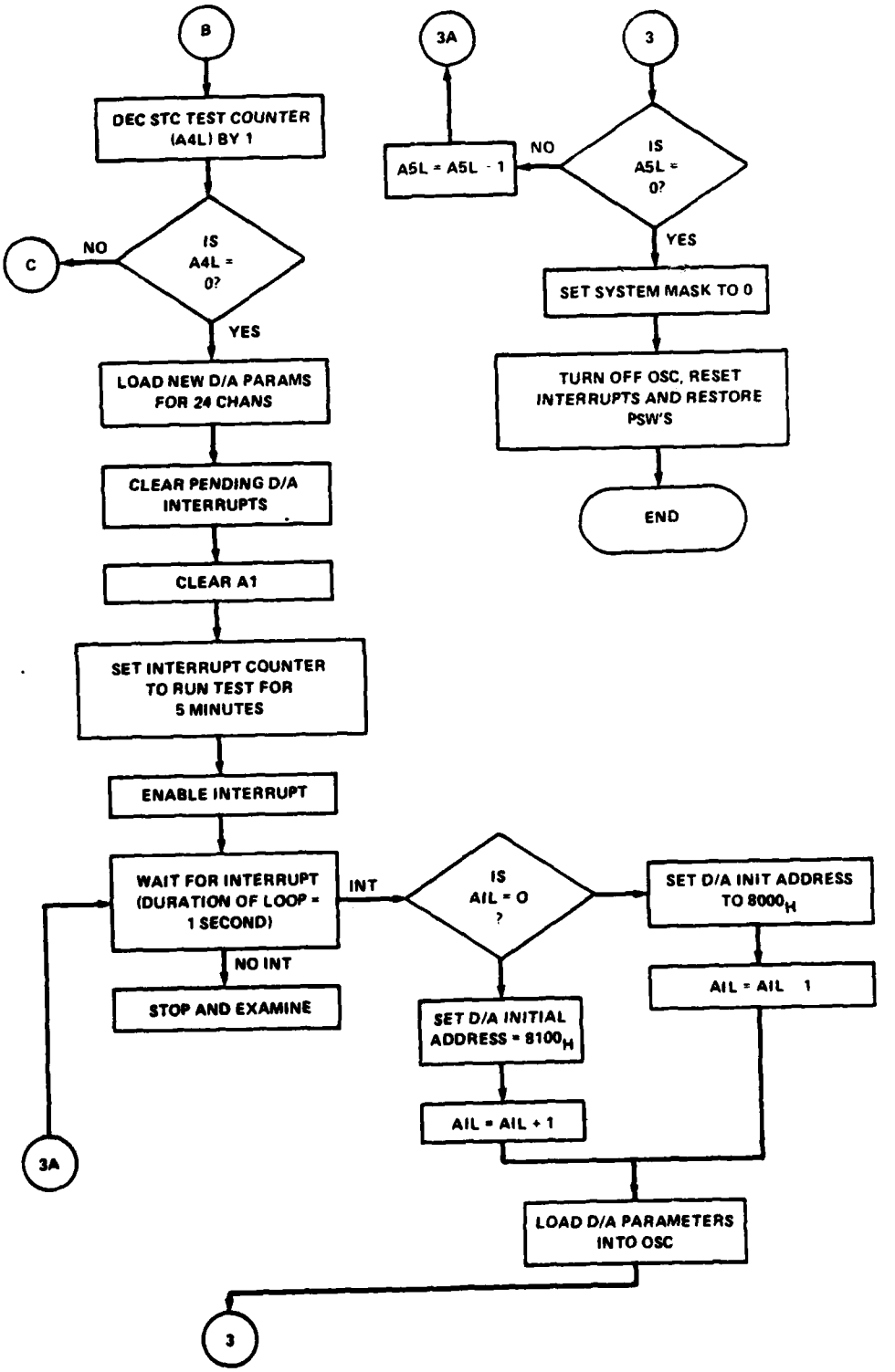


FIGURE 17 BASIC HARDWARE DIAGNOSTICS (3 OF 3)

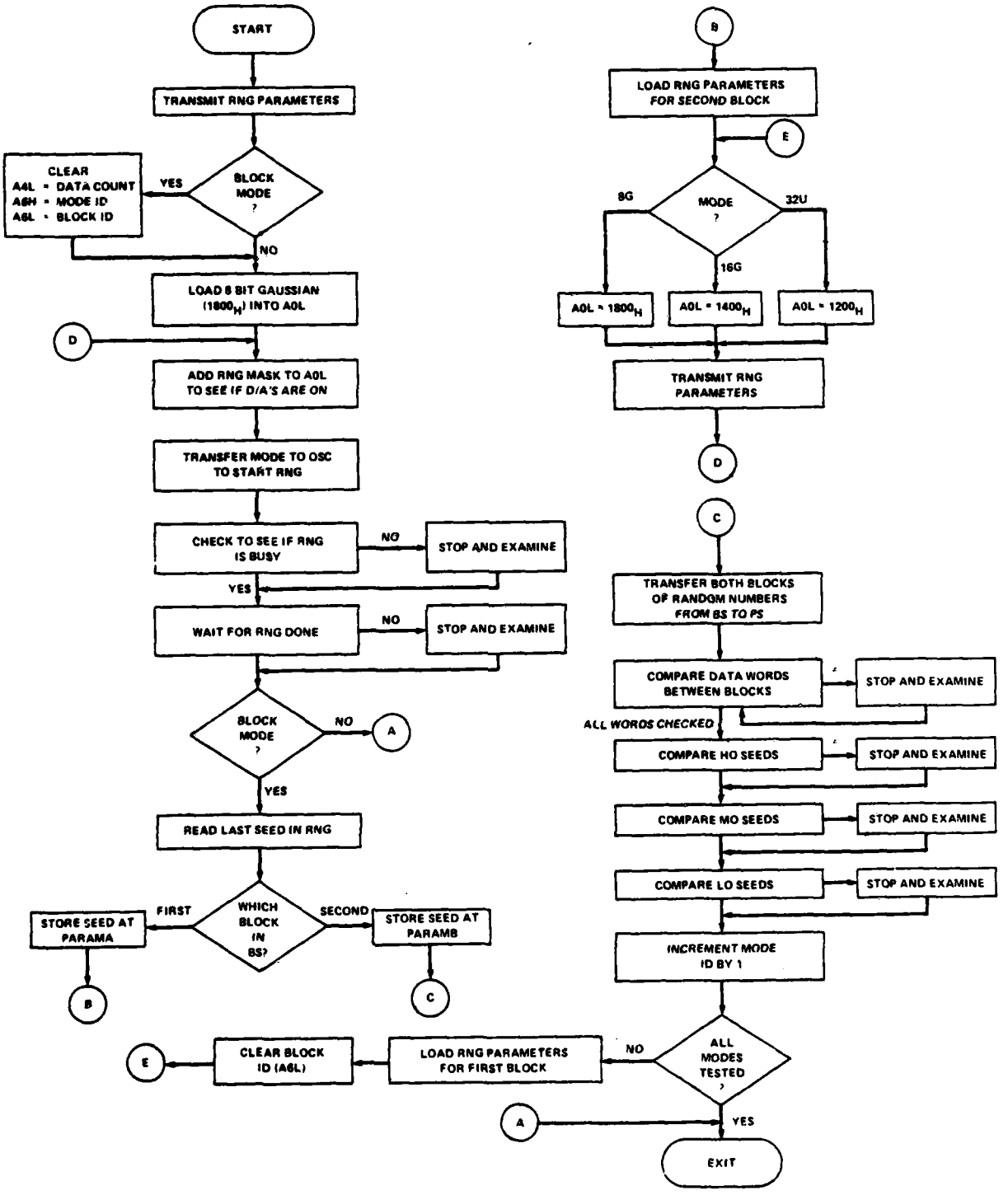


FIGURE 18 SUBROUTINE RNGTES

Bus (EAB) word counter logic is tested next to determine if the counter is reset only when a different OSCBH address is issued. The test sequence is to transfer the High Order Random Number seed, read the AEC STATUS (EXT REGISTER 63) and transfer the Middle and Low Order seeds and read the 39-bit seed back from the RNG for comparison. If an error is detected (seed does not match), the program stops and allows the operator to inspect the registers via the maintenance panel. With the EDB/RTC board verified, the RNG is tested in block mode for each mode in order to see if the data is repeatable. This test is carried out by the subroutine, RNGTES, Figure 18. RNGTES can be run in either block test mode or run mode. An option was added to RNGTES to take into account the operation of the D/A section whenever a block of data is being requested. A variable RNG MASK is used to signify the D/A state whenever RNGTES is called allowing the D/A logic to remain in the same mode whenever the RNG is called. In block testing mode, RNGTES first generates two blocks of data, each 512 full words long. The first mode selected is 8-bit Gaussian. In addition to starting the RNG, RNGTES also checks to see if the RNG is turned on and if the RNG finishes within a reasonable length of time. After the two blocks of data are stored in Bulk Store, the data is then transferred into Program Store for verification. Because the seed was the same for both blocks, the data in one block is compared directly to data in the second block, testing RNG repeatability. As a final check, the last seed is read after each block is generated and compared. This sequence is then repeated for the 16-bit Gaussian and 32-bit Uniform modes. If the block mode is not selected when RNGTES is called, RNGTES will generate only one block of 512 Full Word 8-bit Gaussian random numbers (Run Mode).

Referring to the main flowchart of Figure 17, after the RNG seed has been stored into the RNG and verified, RNGTES is called to exercise the RNG in block mode. The RNG MASK was set to zero in this case because the D/A's were not active when RNGTES was called.

The next section checks the operation of the D/A section of the OSCBH. The method chosen to test this part of the OSCBH requires an oscilloscope to monitor the D/A converter outputs. The data configuration for the D/A buffers is shown in Figure 19.

8000_H	Square Wave
8100_H	Sine Wave
8200_H	Random Numbers
8300_H	Square Wave
8400_H	Sine wave
8500_H	Random Numbers

FIGURE 19 BEGINNING ADDRESS

The square and sine waves are first generated and stored into Program Store and are transferred to Bulk Store in the above pattern. When the square and sine wave patterns have been stored, the RNG is used to fill in the gaps in Bulk Store (RNGTES is called in RUN mode). After all the data has been loaded into Bulk Store, the D/A parameters are loaded into the OSCBH. With the D/A section reading and converting data, the Random Number Generator is tested in the block mode. This case required the RNG MASK to reflect the fact that the D/A subsection was active, and should remain active during RNG transfers. In this way any conflicts between the RNG and D/A sections of the OSCBH are tested. After these tests are finished, Storage Transfer Controller conflicts are monitored by performing Bulk Store to Program Store transfers and vice-versa while the D/A's are active. The data transfer path between Program Store and Bulk Store is tested by first transferring the square and sine stored in Program Store to Bulk Store and then reading the data into Program Store from Bulk Store. With these two blocks of data, a comparison is made on each element. This transfer and block testing is performed five times.

The final set of tests are with the D/A section of the OSCBH only. This section activates all 24 D/A channels of the OSCBH and checks the OSCBH interrupt. A new set of parameters is first loaded into the OSBCH to enable all the D/A channels. The pending OSCBH interrupts are then cleared in the AN/UYS-1 queue, the PSW System Mask is changed to allow interrupts and a waiting loop is entered. The waiting loop is programmed to wait for an interrupt until a maximum of one second has elasped. If no interrupt has occurred, the program is stopped. When an interrupt is received, the D/A initial address is changed from either 8100 to 8000 or 8000 to 8100. This change in the initial address causes the waveform to flip-flop during each interrupt received. In this way, an oscilloscope can monitor any of the D/A channels and determine if the interrupt is being sent by the OSCBH and received by the AN/UYS-1. The waveforms can be found in Appendix E. A total of 1800 interrupts are processed by the software, allowing the operator approximately five minutes to check all 24 D/A channels with an oscilloscope. When an interrupt is not received, two things indicate a failure, the waveform on the oscilloscope does not change and the program stops (indicated on the maintenance panel). This test constitutes the final test after which the program terminates by shutting down the OSCBH, clearing any pending interrupts and finally restoring the PSW's to their initial values in locations $7C_H$ and $6A_H$.

The source program of the diagnostic software is found in Appendix F.

CHAPTER 6

CONCLUSIONS

This report described a particular prototype Output Signal Conditioner Basic Hardware (OSCBH) configuration for a particular Digital Acoustic Sensor Simulator (DASS) system. The design requirements given at the beginning of this report were met by this OSCBH. Also, this unit was constructed using an earlier in-house unit as a model. In the process of transferring the in-house technology to the unit described, a few improvements were made to increase the reliability and performance of the OSCBH. The improvements made were:

a. The substitution of more reliable connectors for transferring the ribbon cable to the OSCBH backplane.

b. Addition of forced air cooling.

c. The substitution of Digital-to-Analog Converters requiring less power.

In the implementation of this unit, the method of extending the ECDB and EDB from the AN/UYS-1 to the OSCBH using five foot lengths of ribbon cable with the alternating ground arrangement was found to provide an acceptable signal waveform at both terminations. This was all the more significant because of the 10 megahertz bus operation for the EDCB. The interface debugging only required adjusting the timing and pulse width of certain control signals to compensate for the transmission line effects observed.

Performance of the separate modules within the OSCBH was assessed during construction and debug. The D/A section was easily checked by using an oscilloscope to determine accuracy and continuity (photographs of the observed waveforms can be found in Appendix E). To verify the performance of the Random Number Generator, a simple histogram program was written to put the samples into bins and then display the results. Three plots from the histogram program are given in Figures 20, 21, and 22. Figure 20 shows the 32-bit uniform random number distribution, Figure 21, the 8-bit Gaussian distribution and Figure 22 the 16-bit Gaussian distribution.

The improvements and future effort for the OSCBH will be aimed at three principle areas. The first area of effort will be directed toward expanding the number of D/A channels available from 24 to 32. This entails converting the Augat^{R} D/A boards to a printed circuit board type layout in order to fit more boards into the Augat^{R} enclosure. The second area will consist of adapting the OSCBH to accommodate new functions. One of these functions will include an Analog to Digital (A/D) unit, which will support 32 input channels. The schematics included with this report show the control logic implemented in this

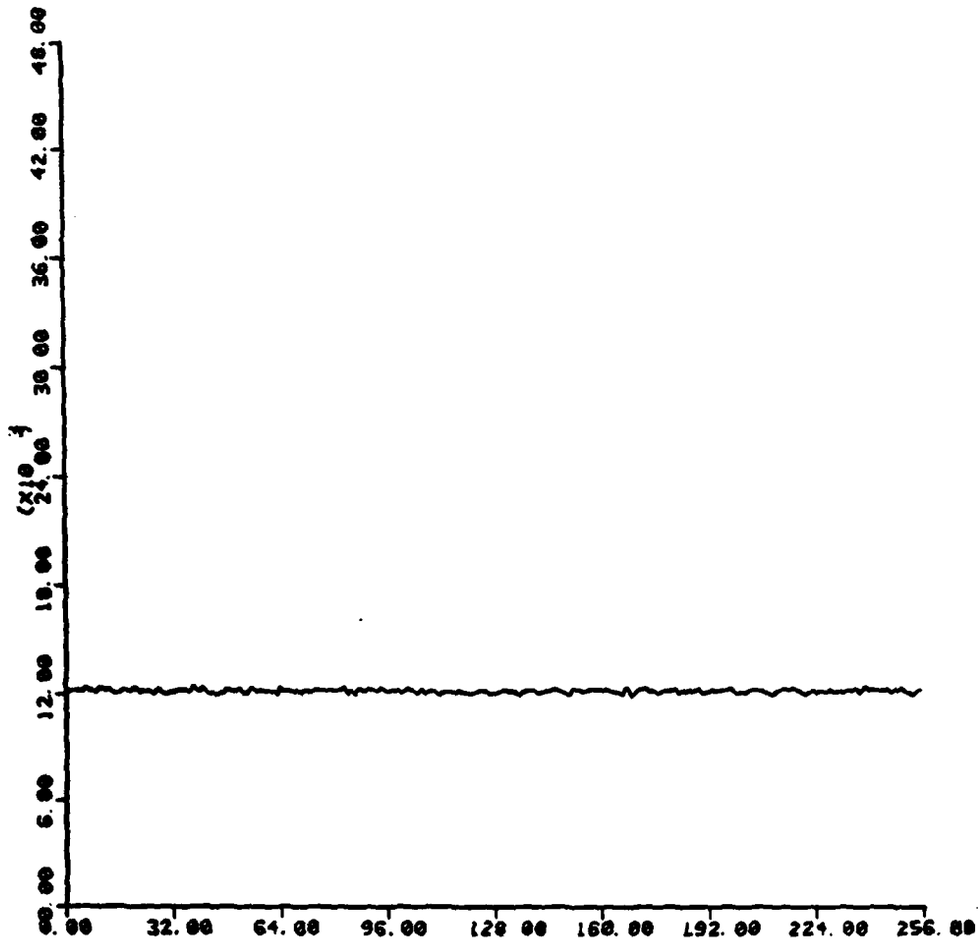


FIGURE 20 32 BIT UNIFORM MODE HISTOGRAM

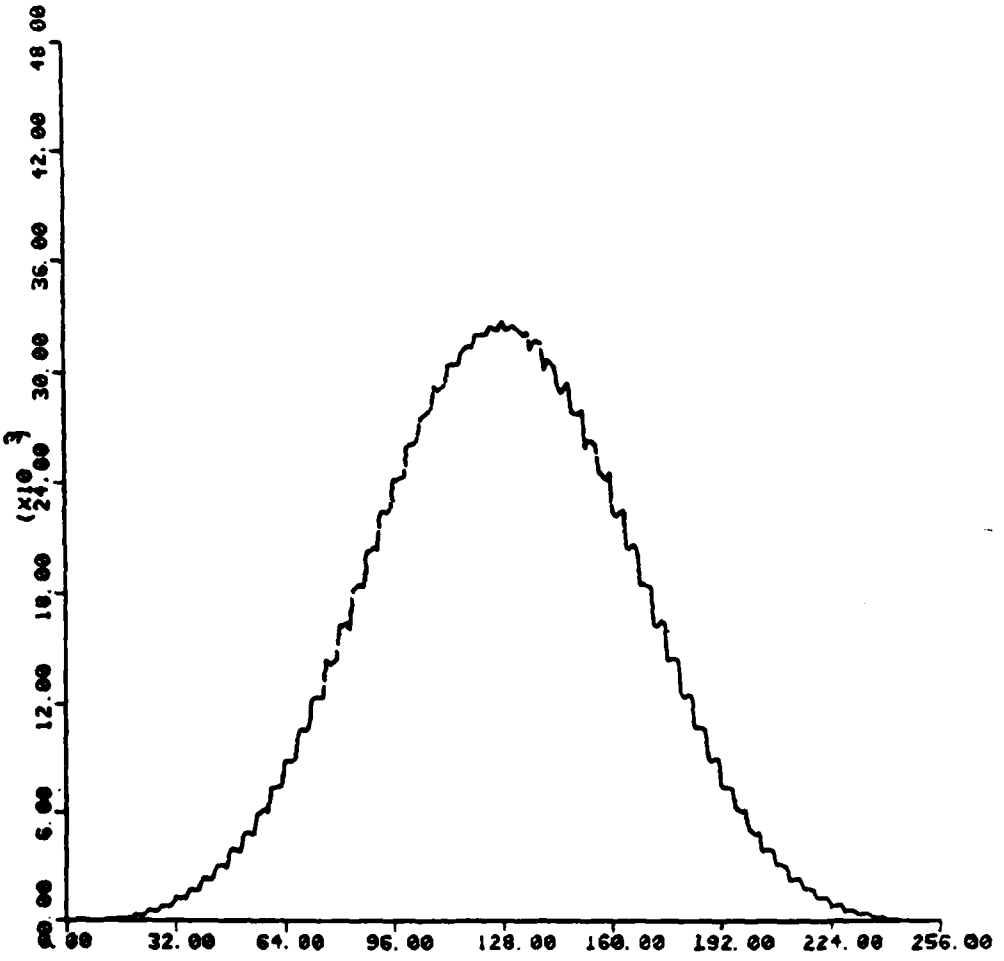


FIGURE 21 8 BIT GAUSSIAN MODE HISTOGRAM

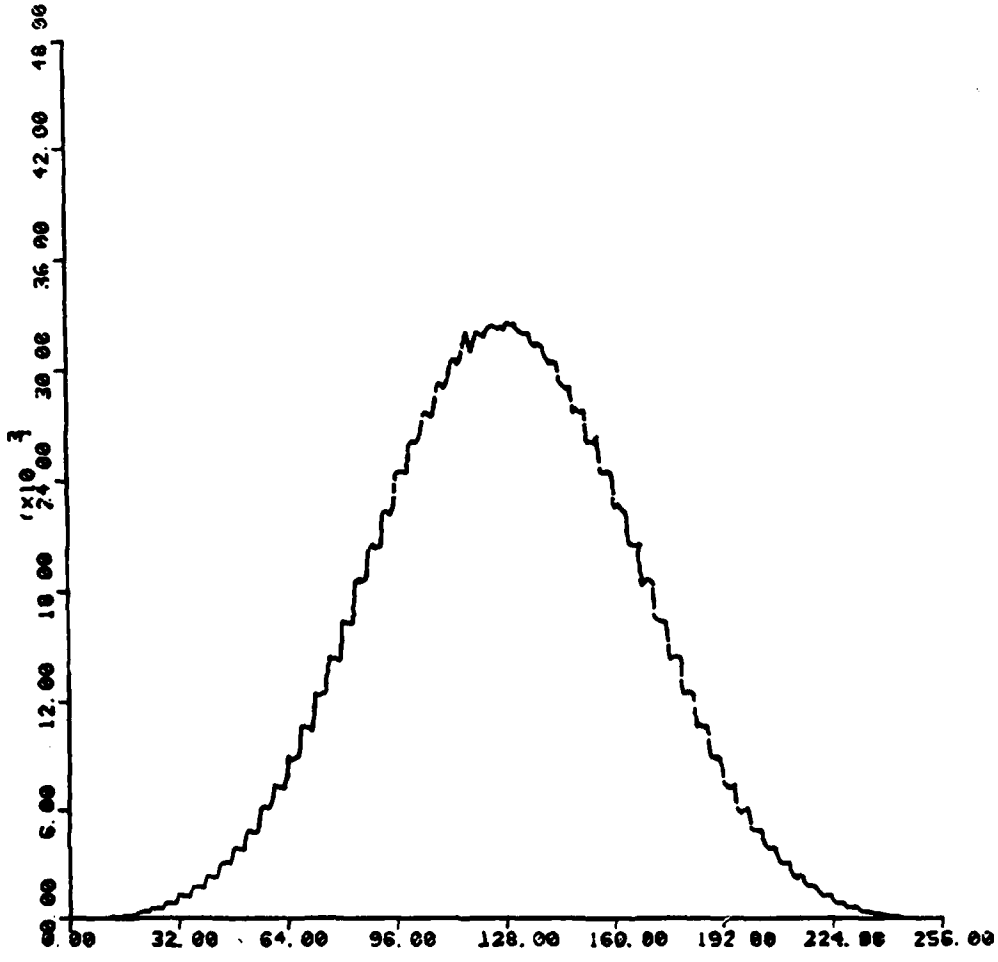


FIGURE 22 16 BIT GAUSSIAN MODE HISTOGRAM

unit for future operation and integration with the A/D circuit boards. The final area of effort will deal with interfacing the OSCBH to the AN/UYS-1. A new interface page is being designed and implemented for future AN/UYS-1 STM units which will be capable of supporting high speed transfers to and from the AN/UYS-1 and an external unit. The design effort of the OSCBH would then be directed toward this new interface.

APPENDIX A

OUTPUT SIGNAL CONDITIONER
BASIC HARDWARE SCHEMATICS

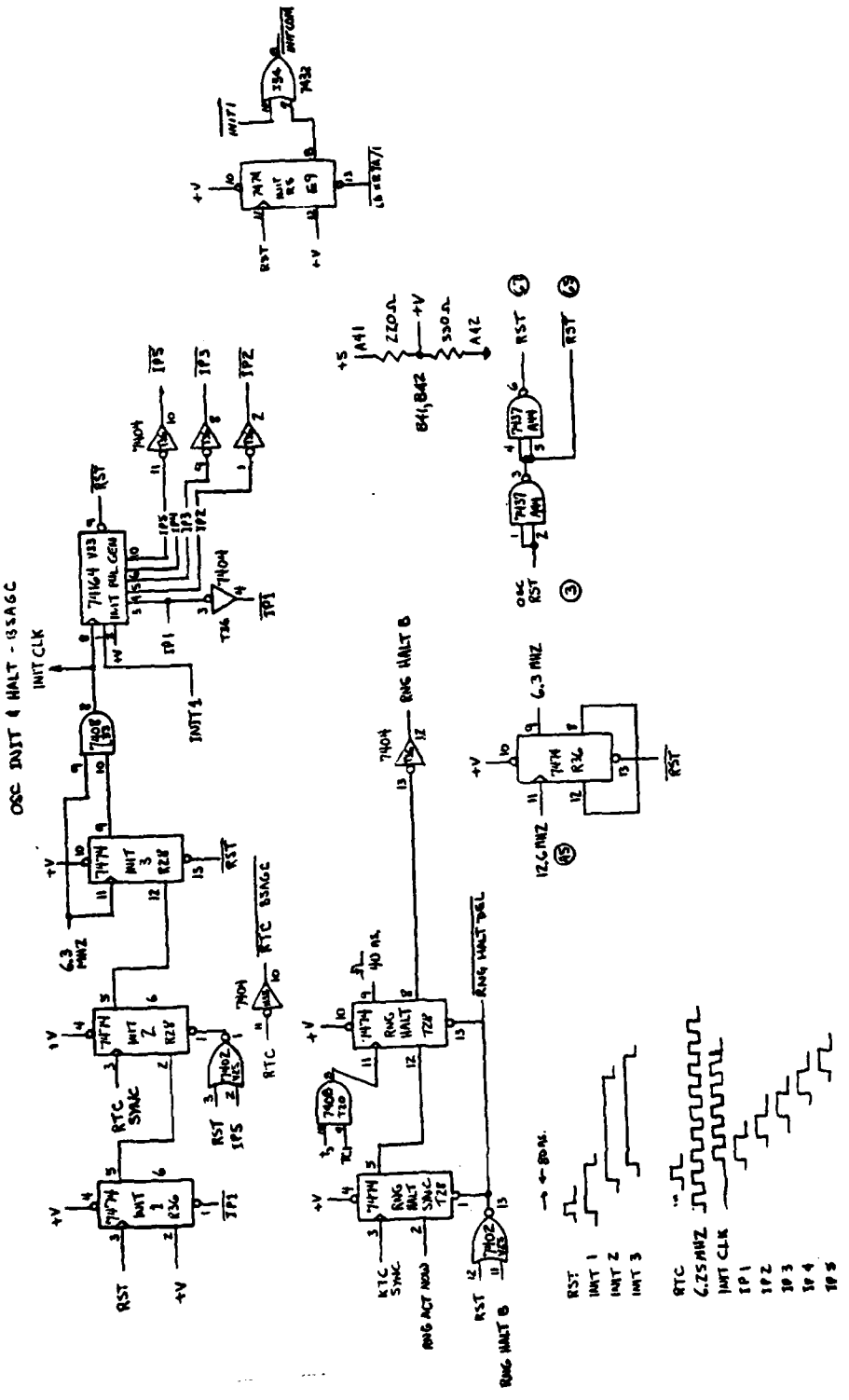


FIGURE A-1 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

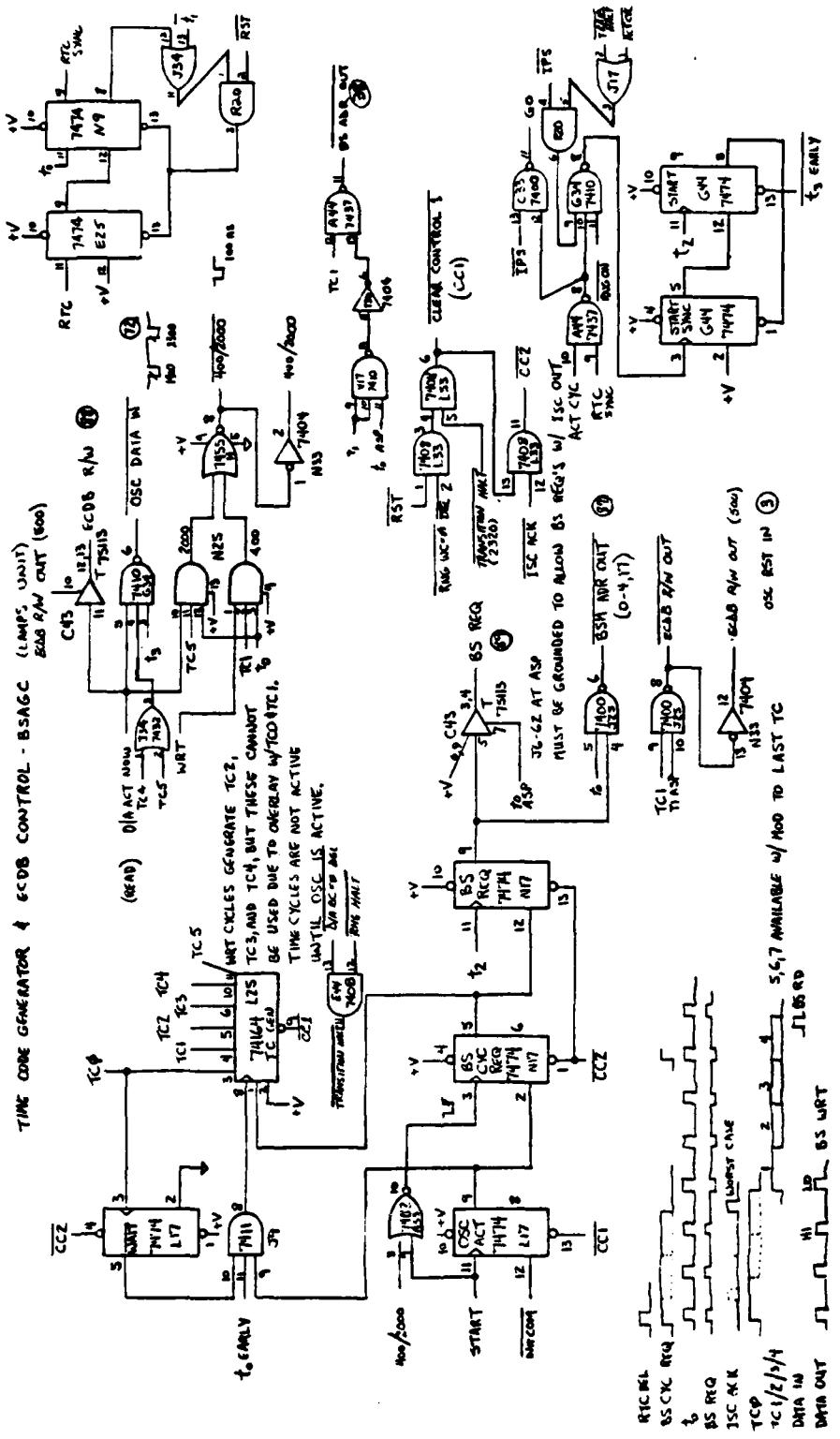


FIGURE A-2 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

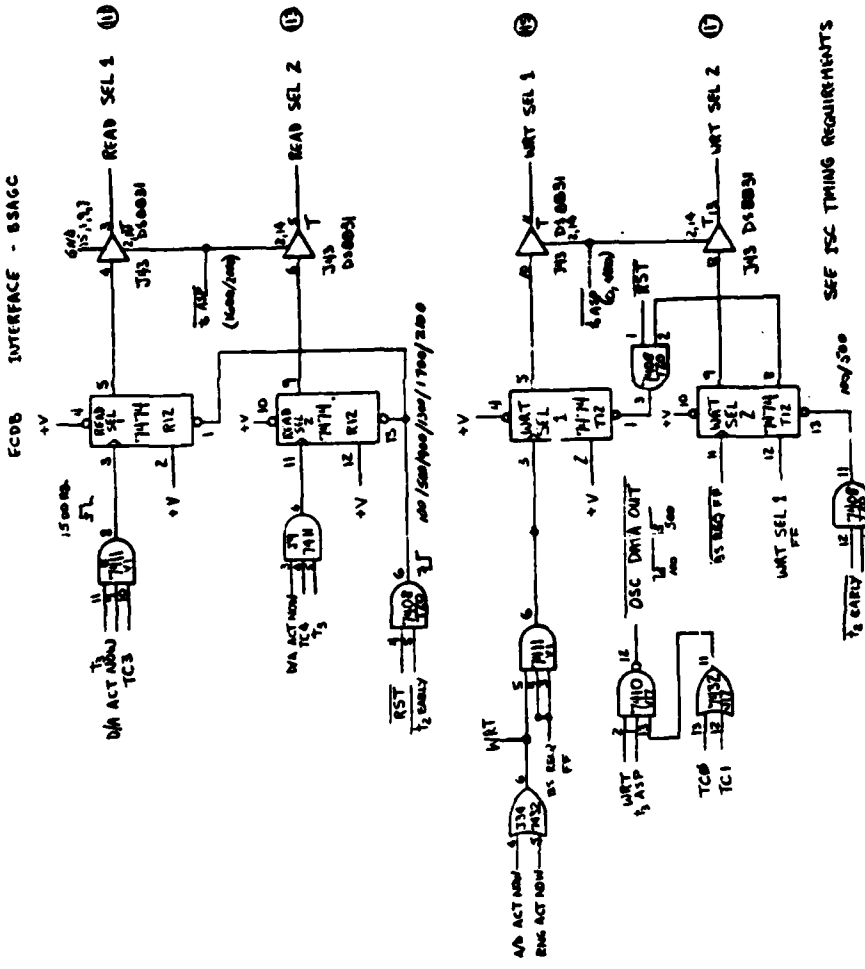


FIGURE A-3 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

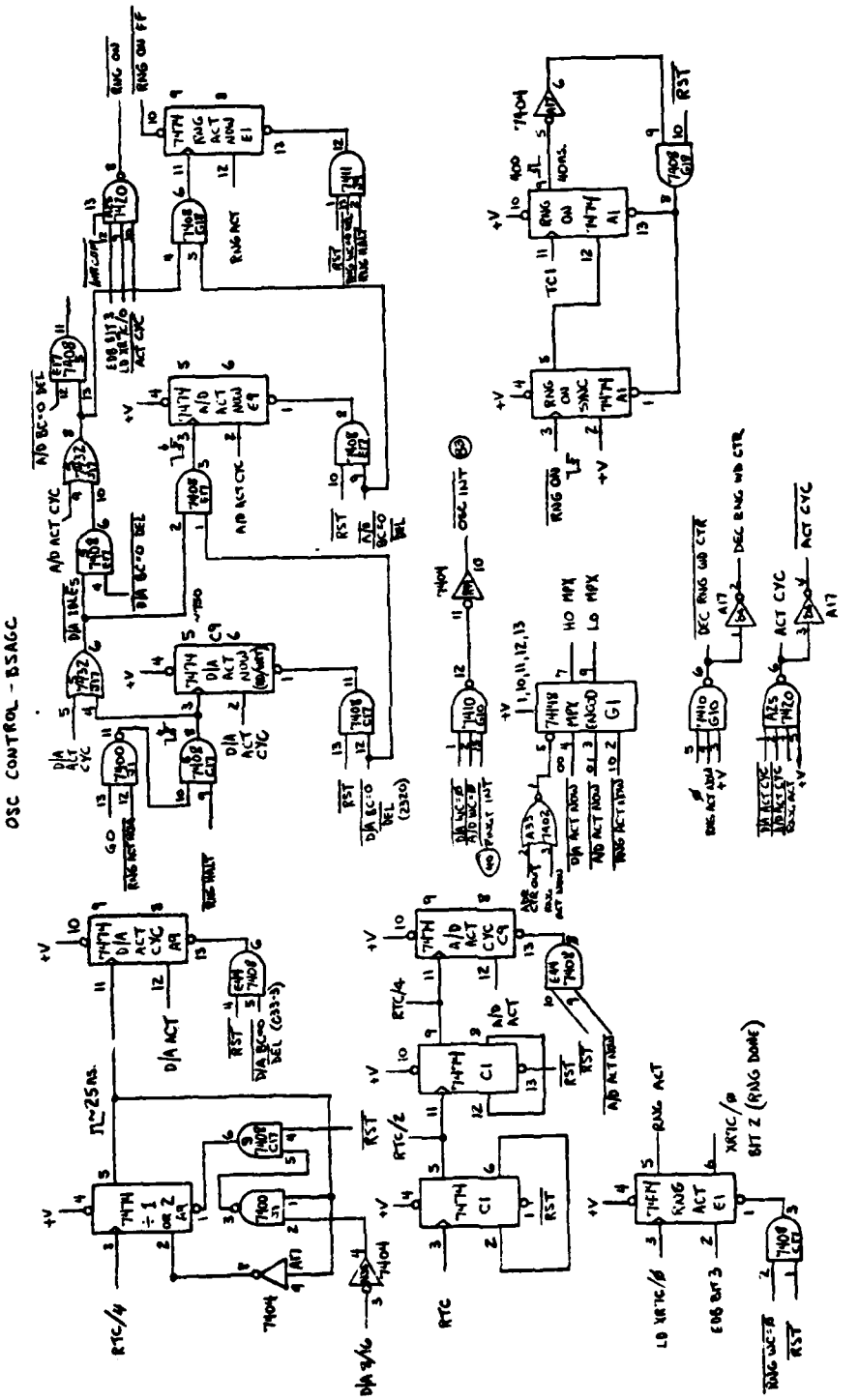


FIGURE A-4 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

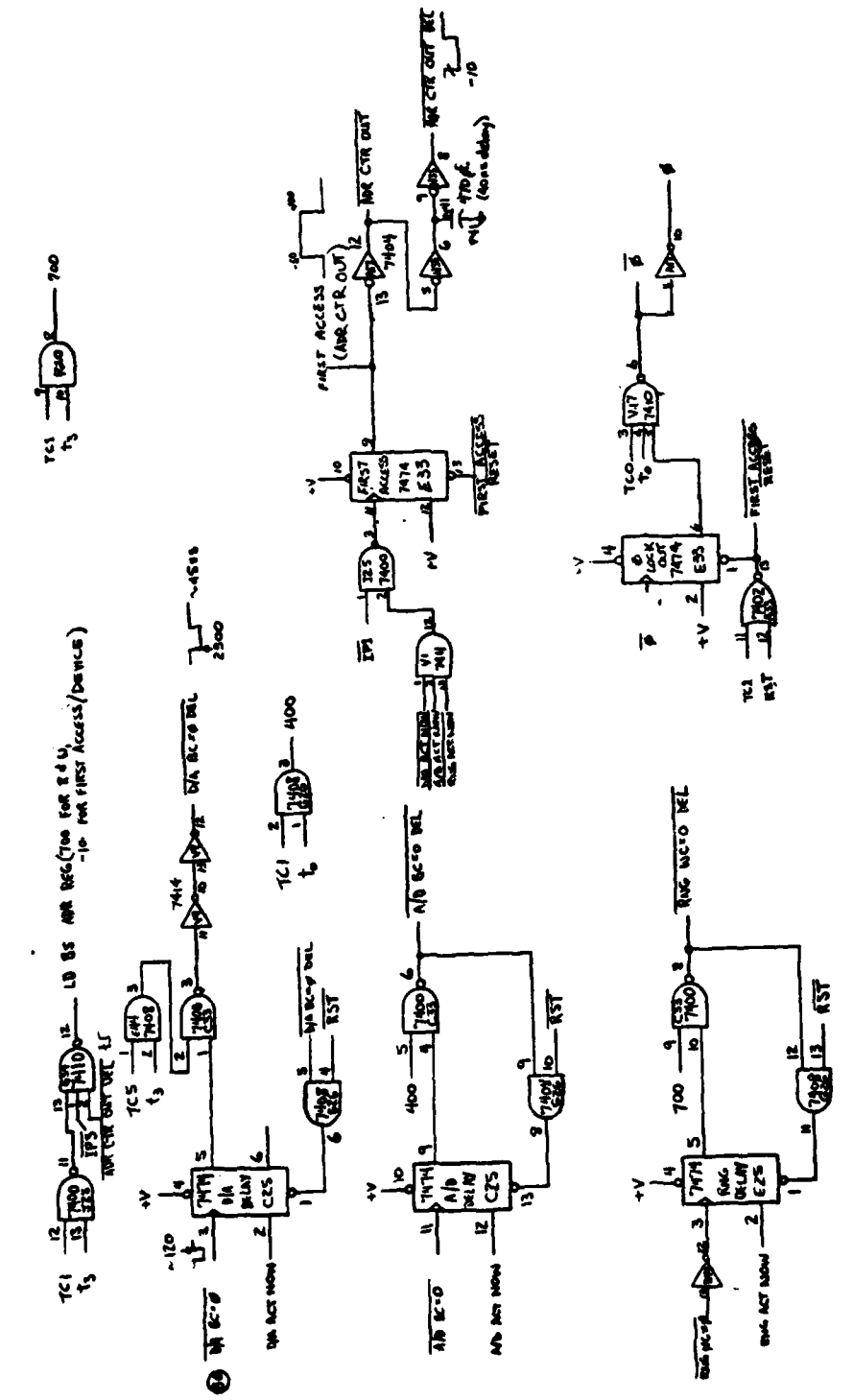


FIGURE A-5 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

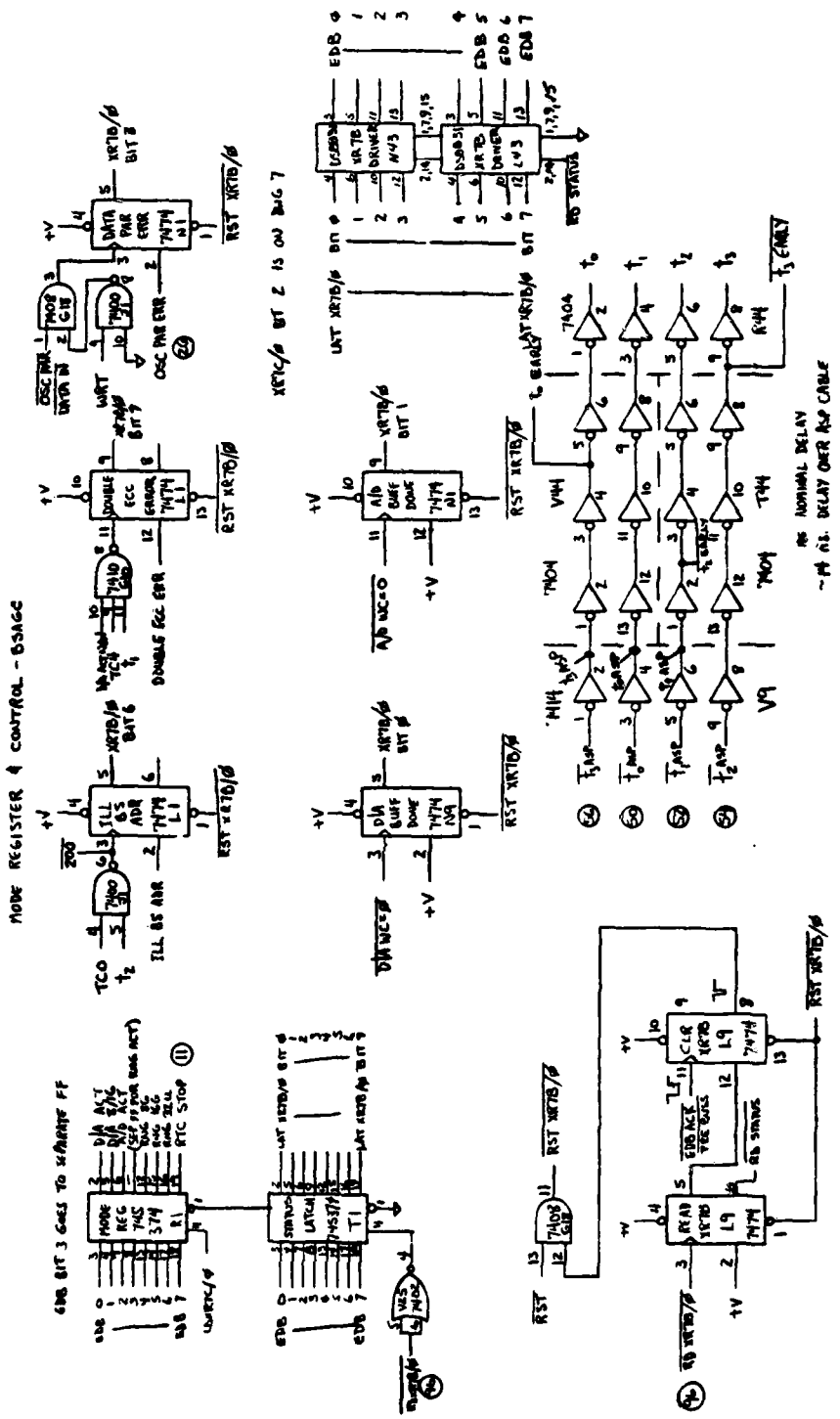


FIGURE A-6 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

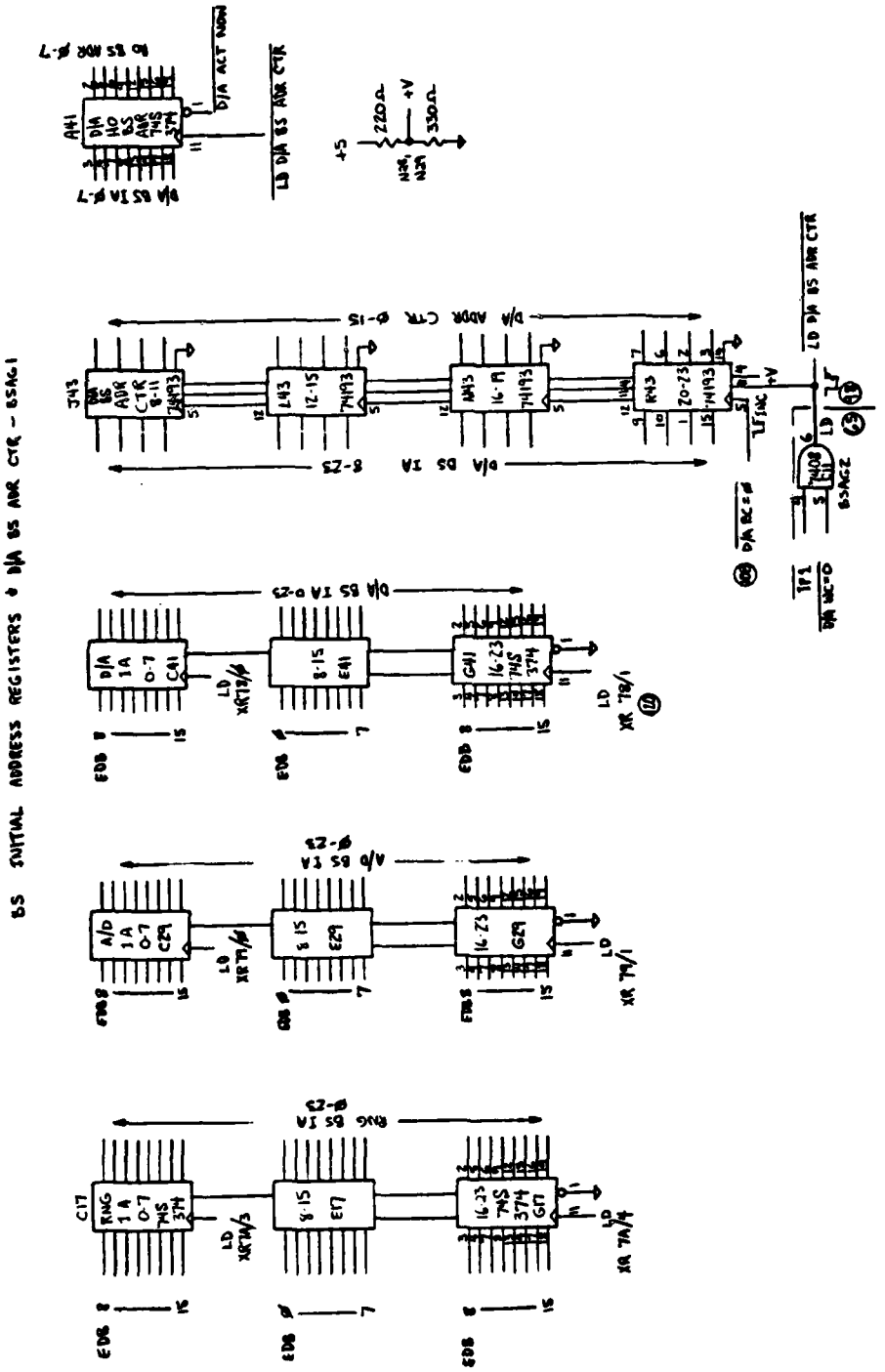


FIGURE A-7 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

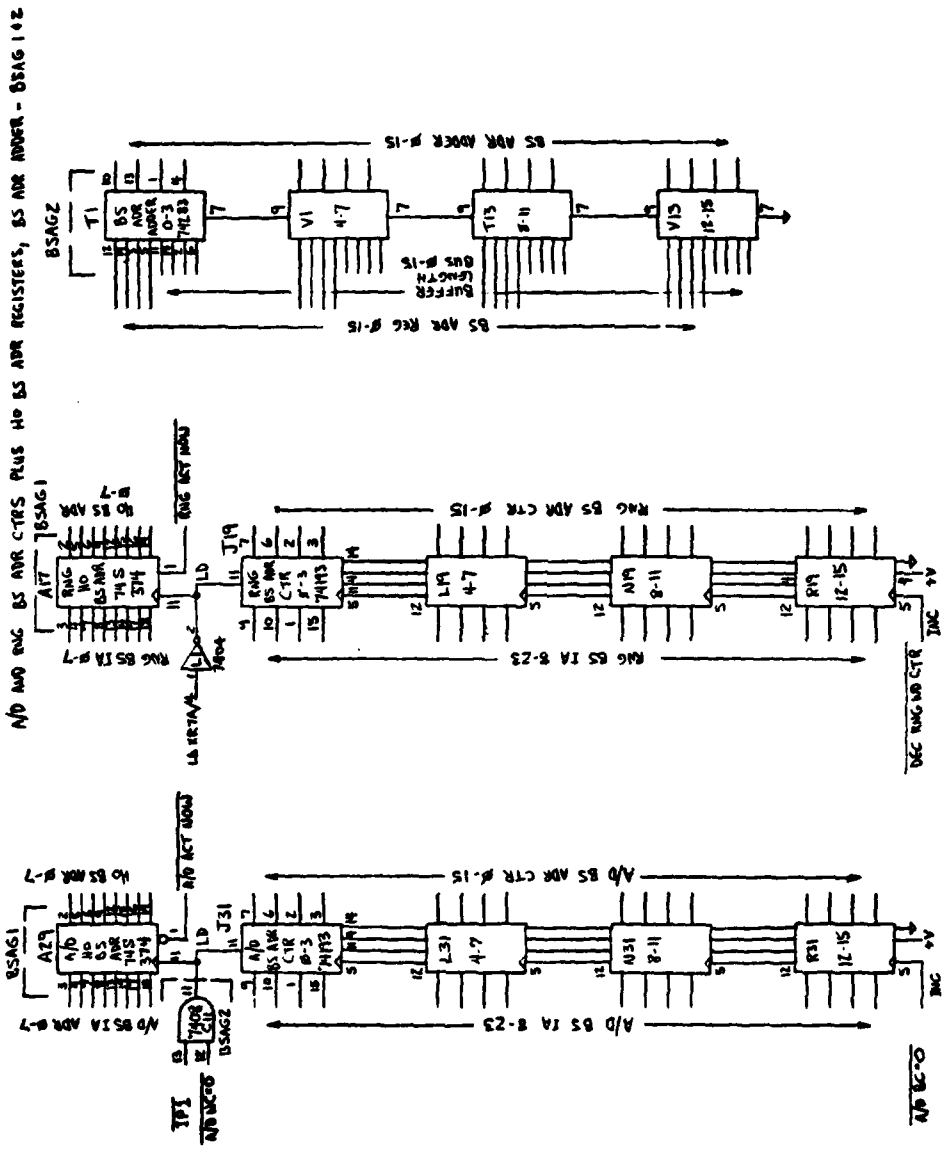


FIGURE A-8 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

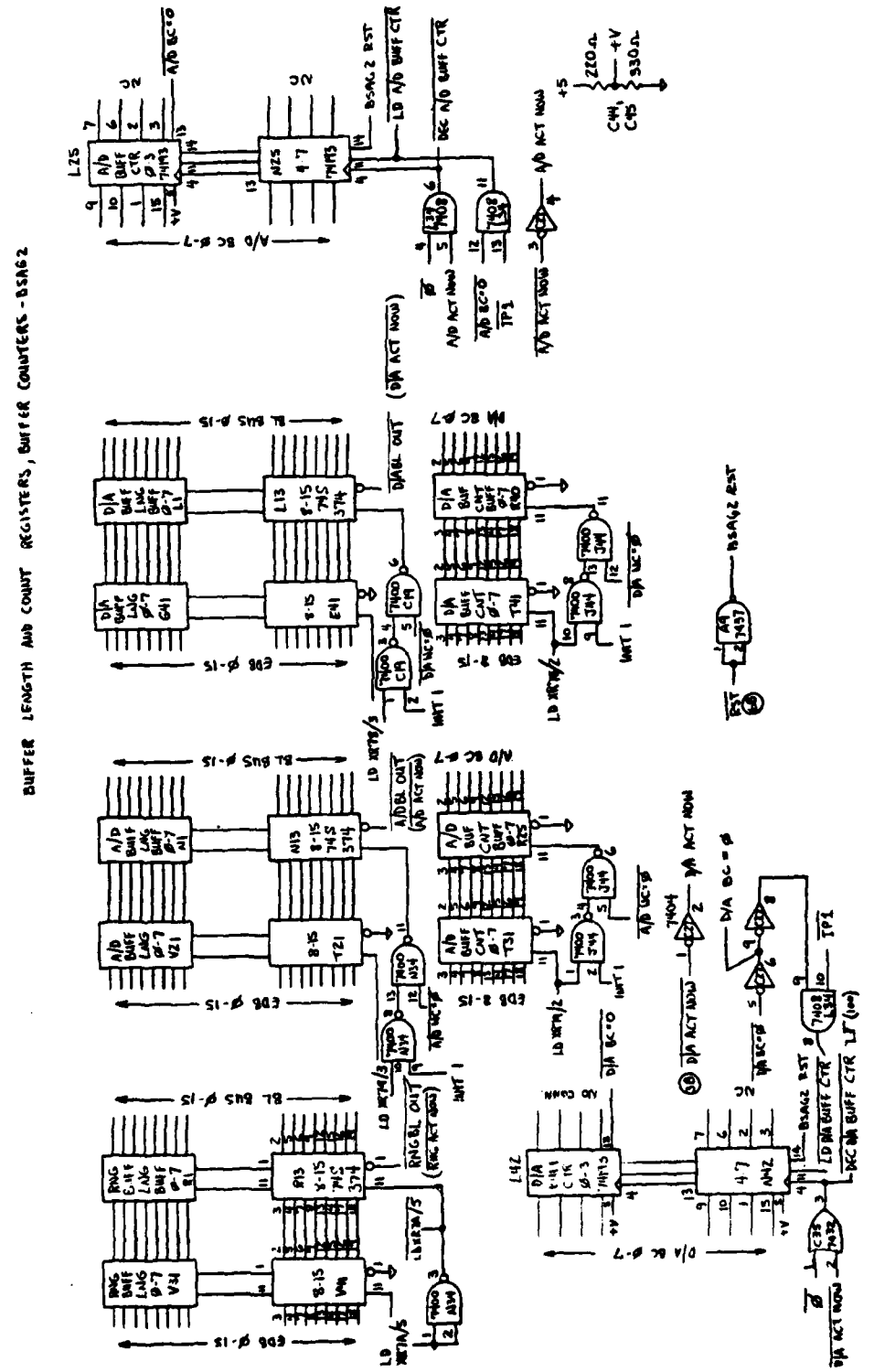


FIGURE A-9 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

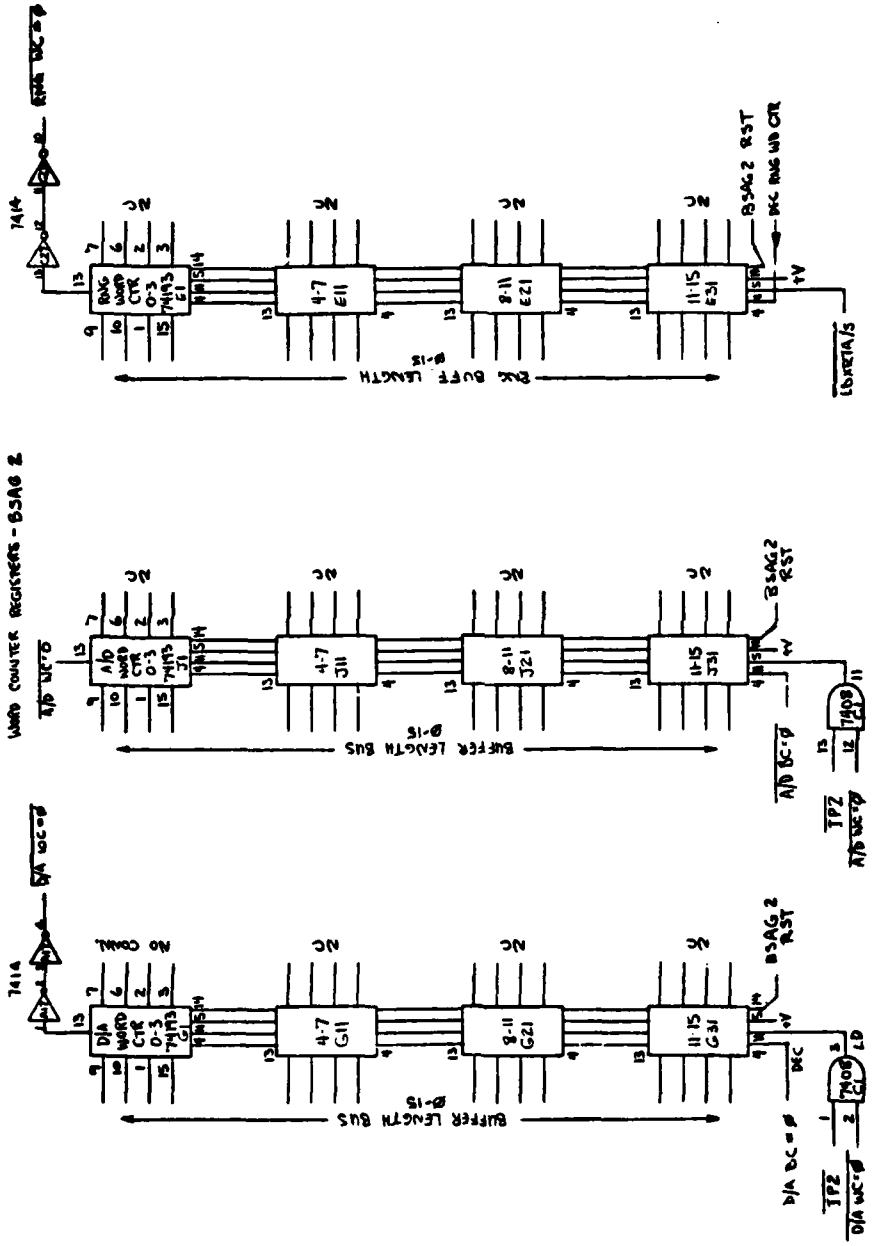


FIGURE A-10 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

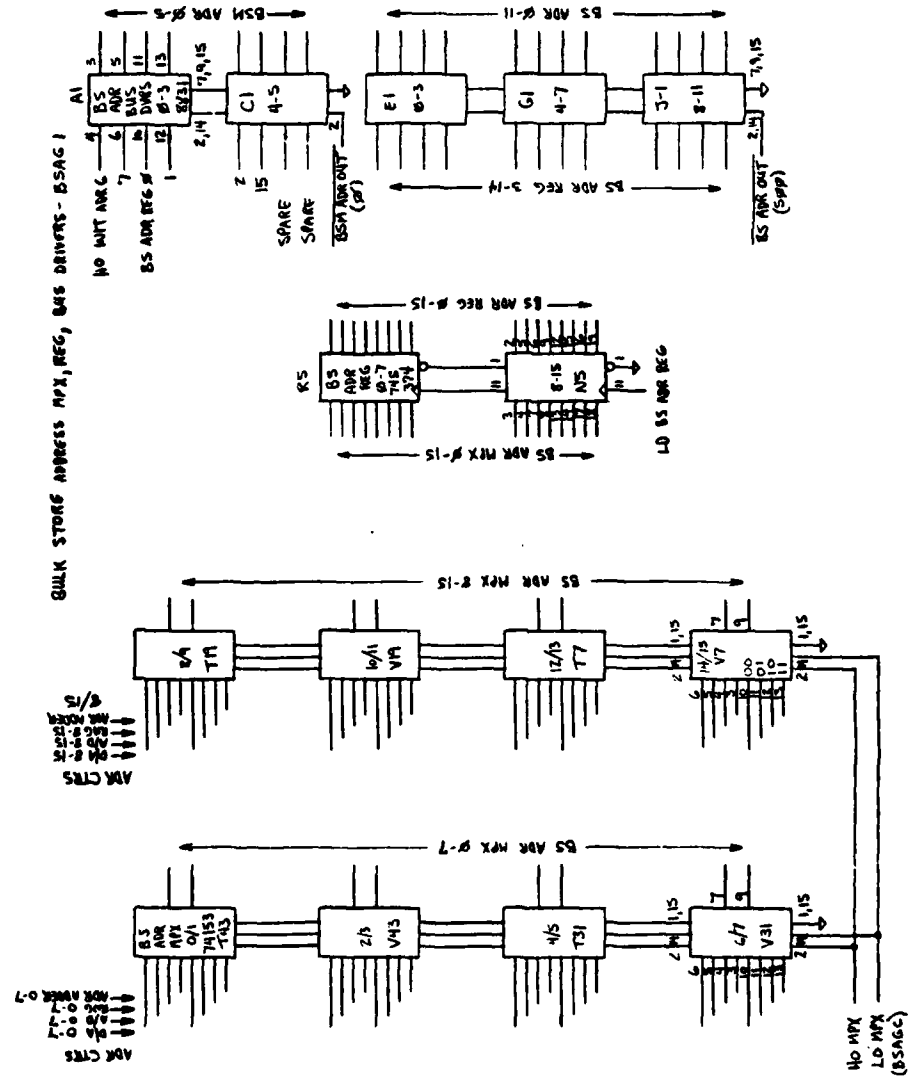


FIGURE A-11 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

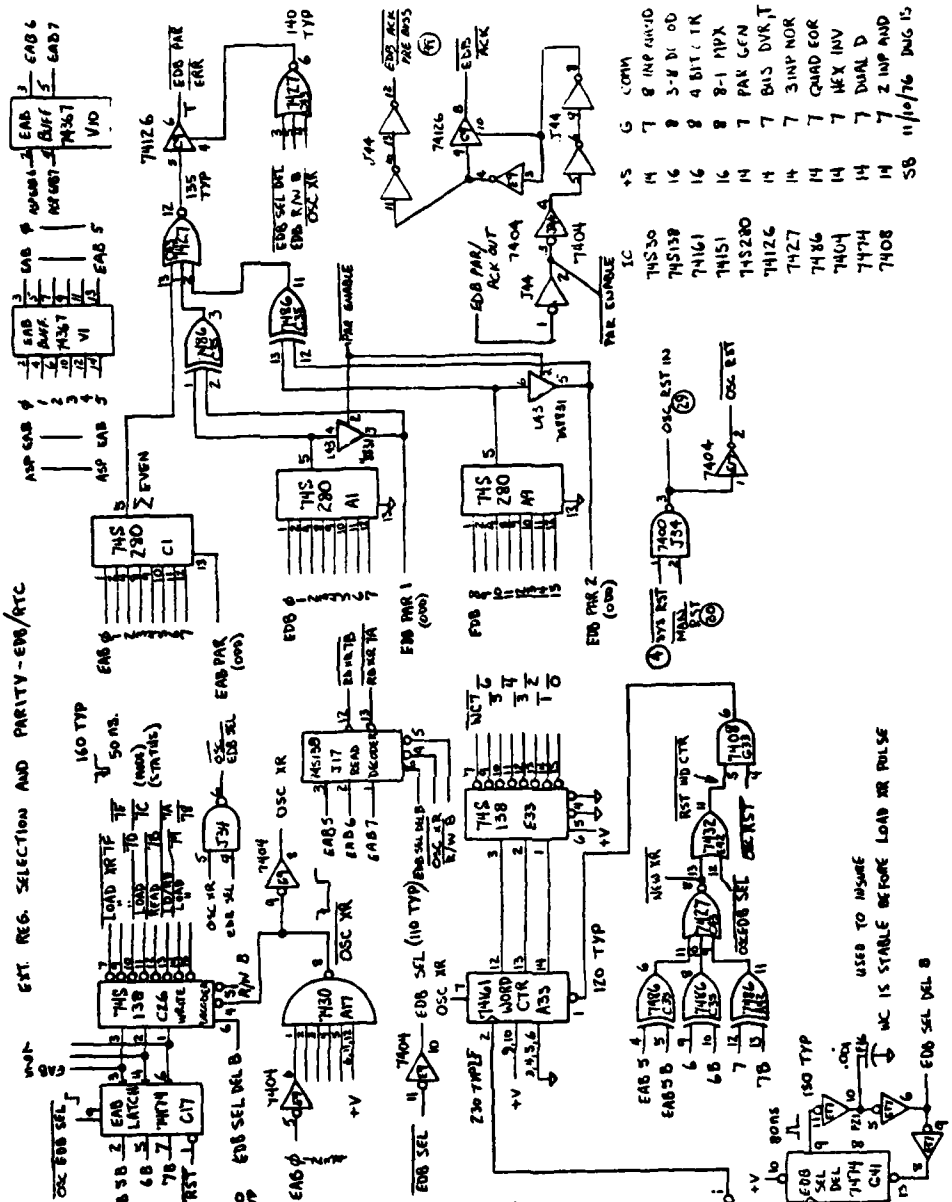


FIGURE A-12 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

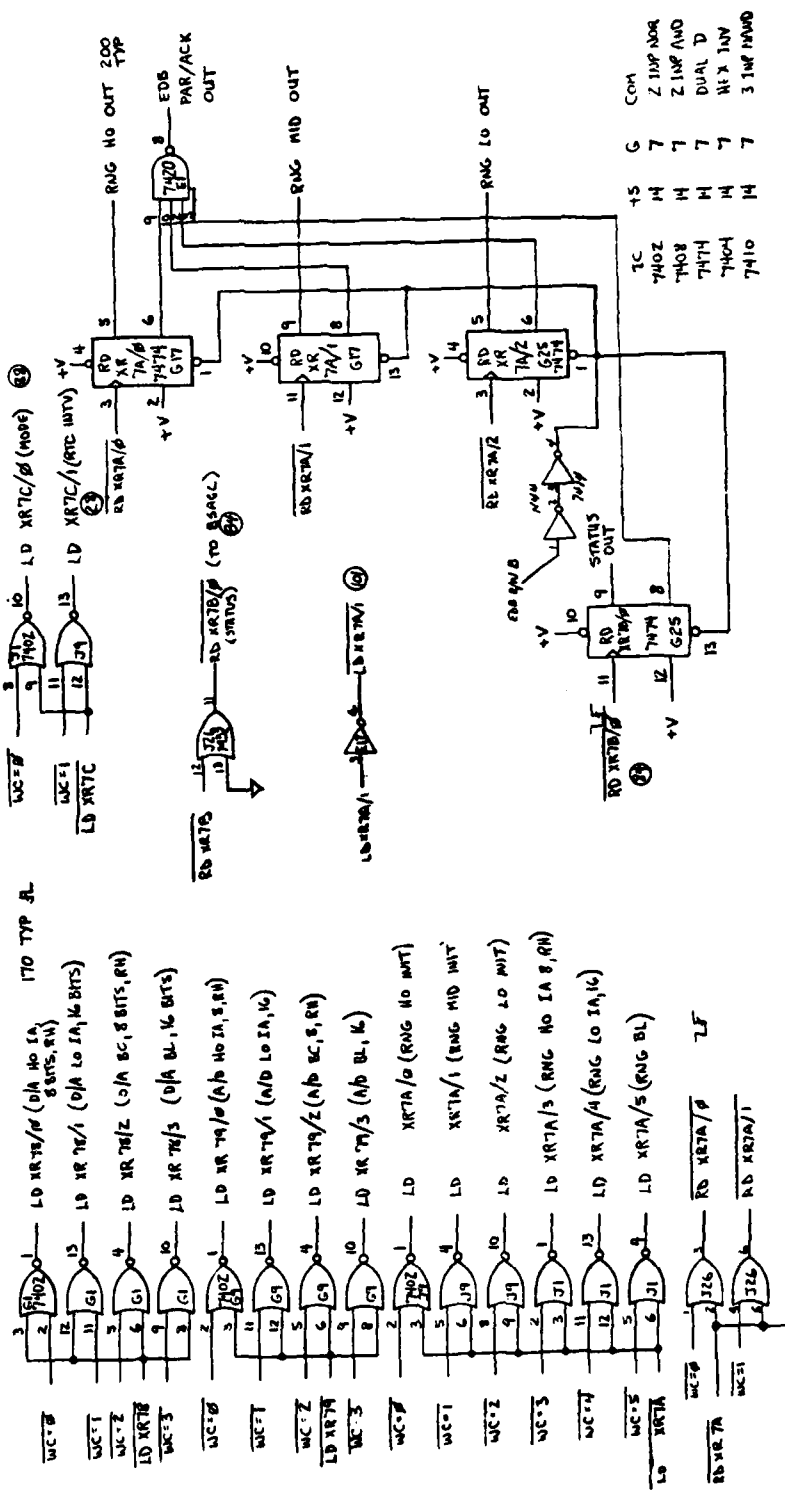


FIGURE A-13 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

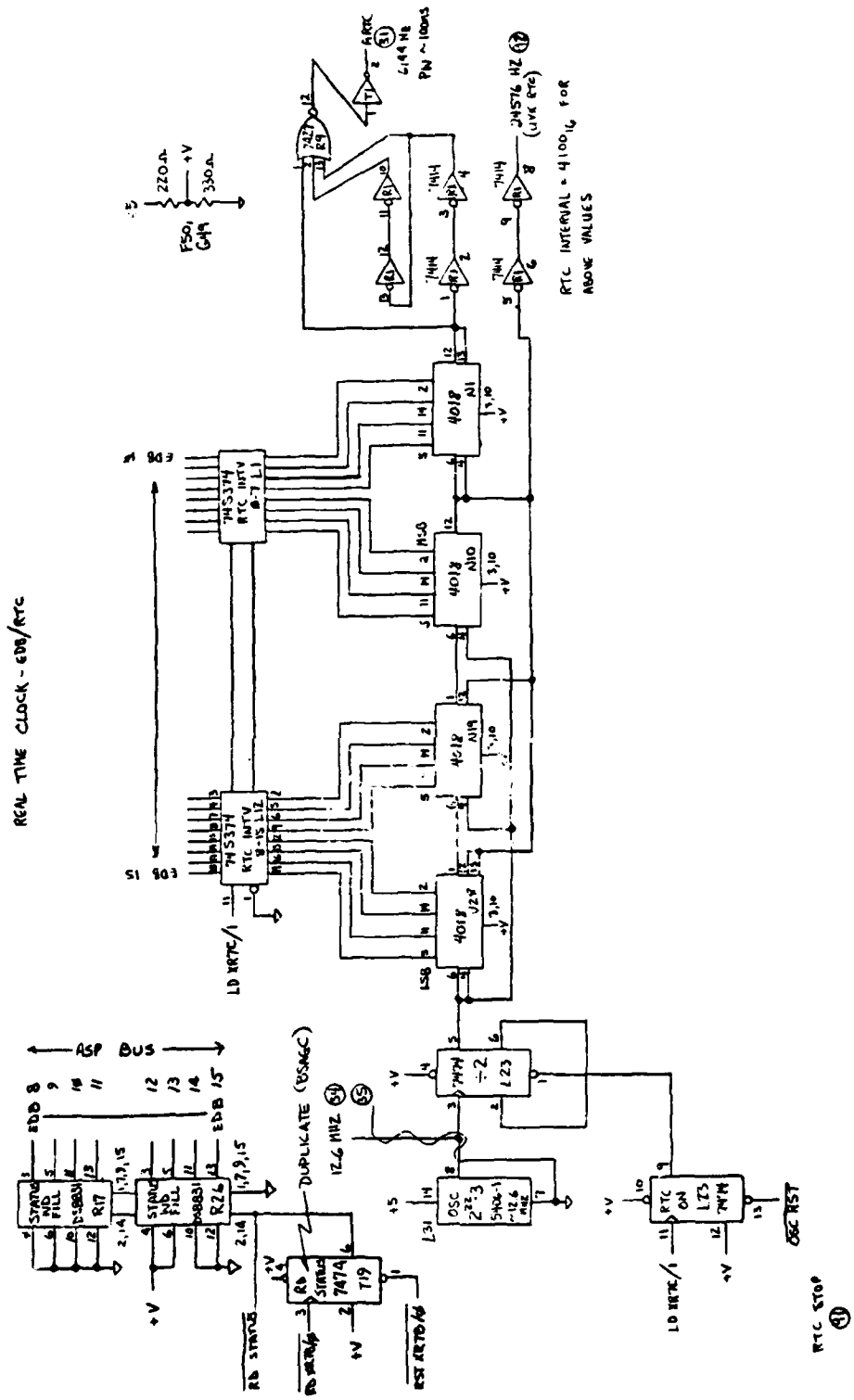


FIGURE A-14 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

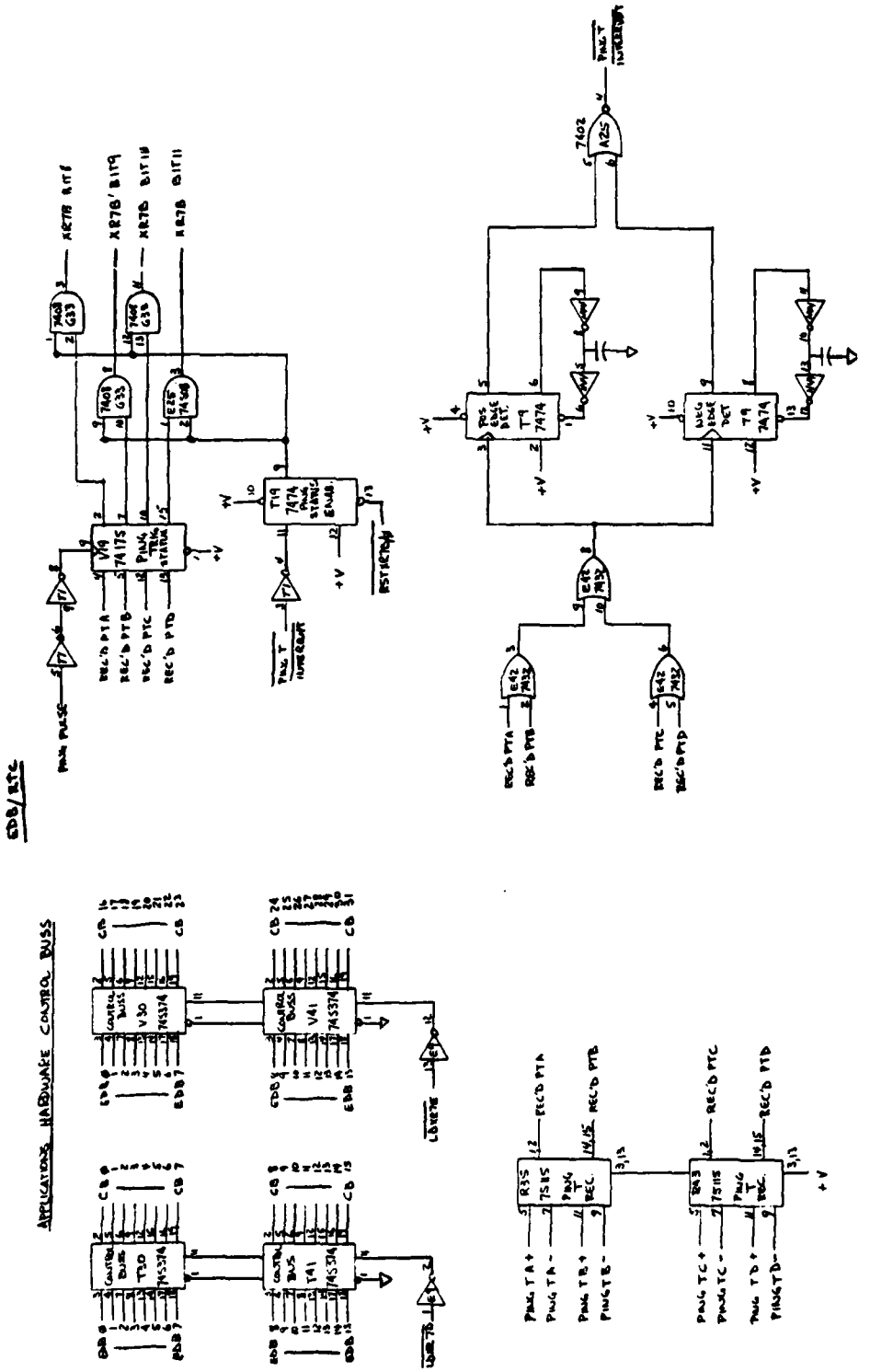


FIGURE A-15 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

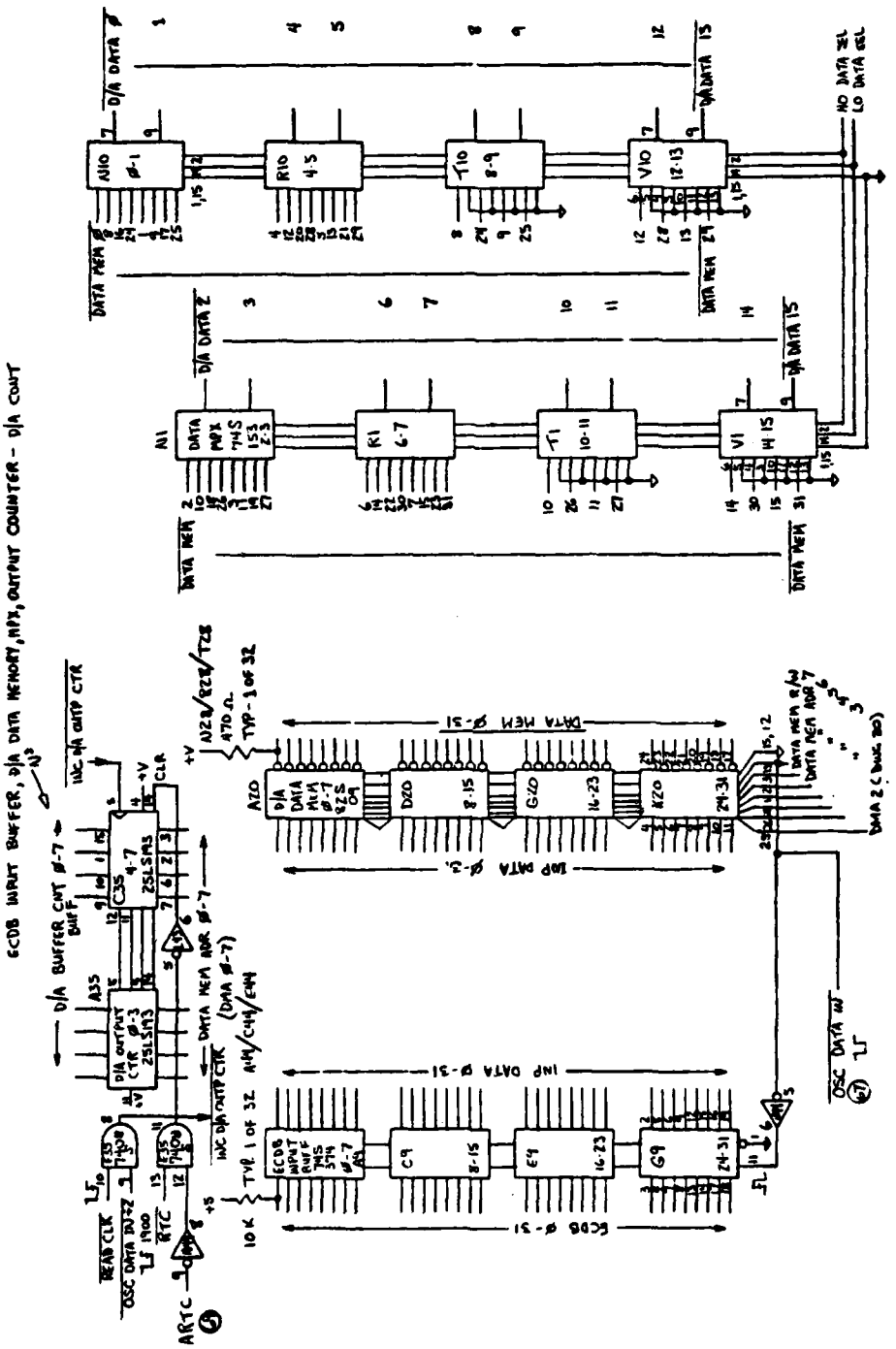


FIGURE A-16 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

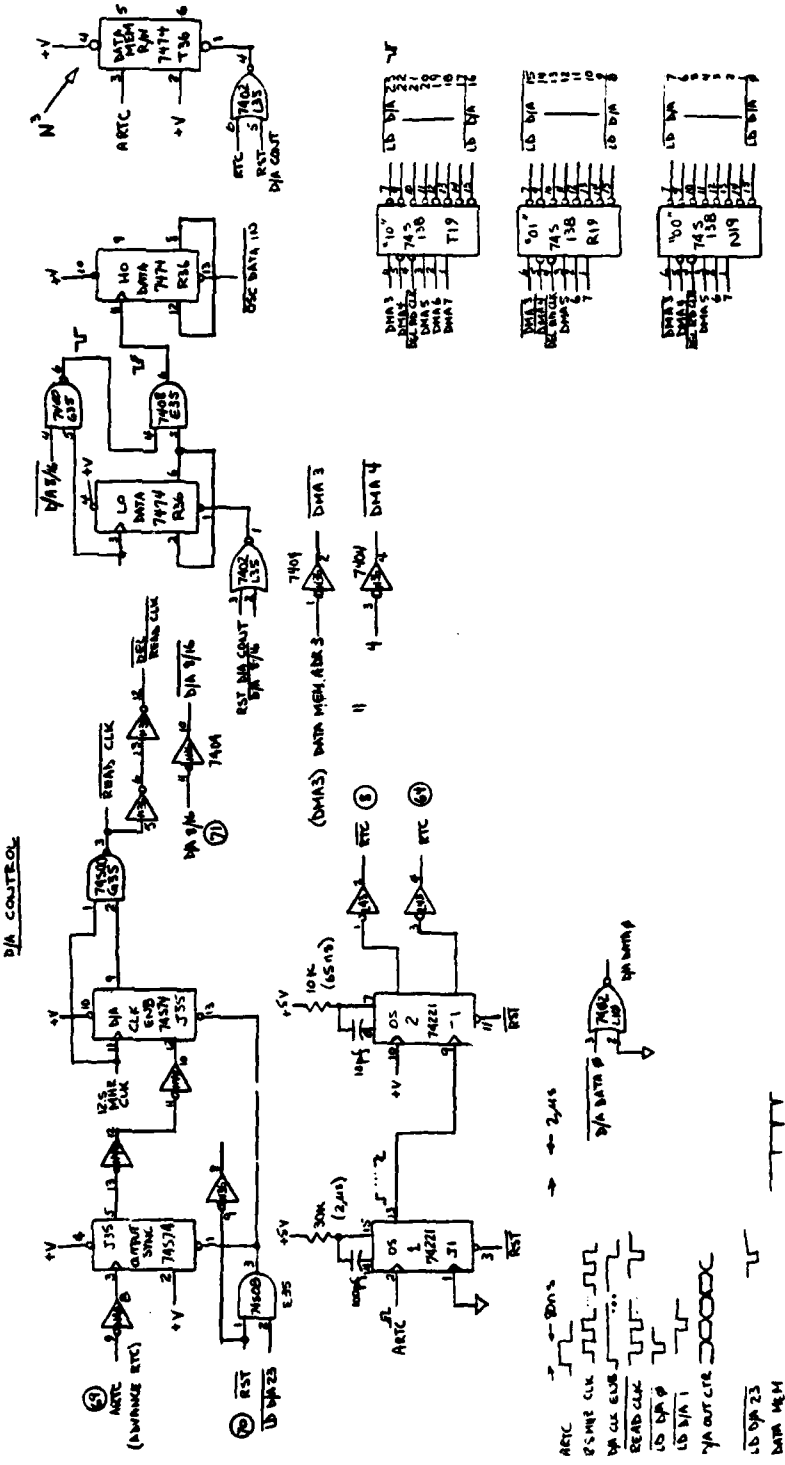


FIGURE A-17 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

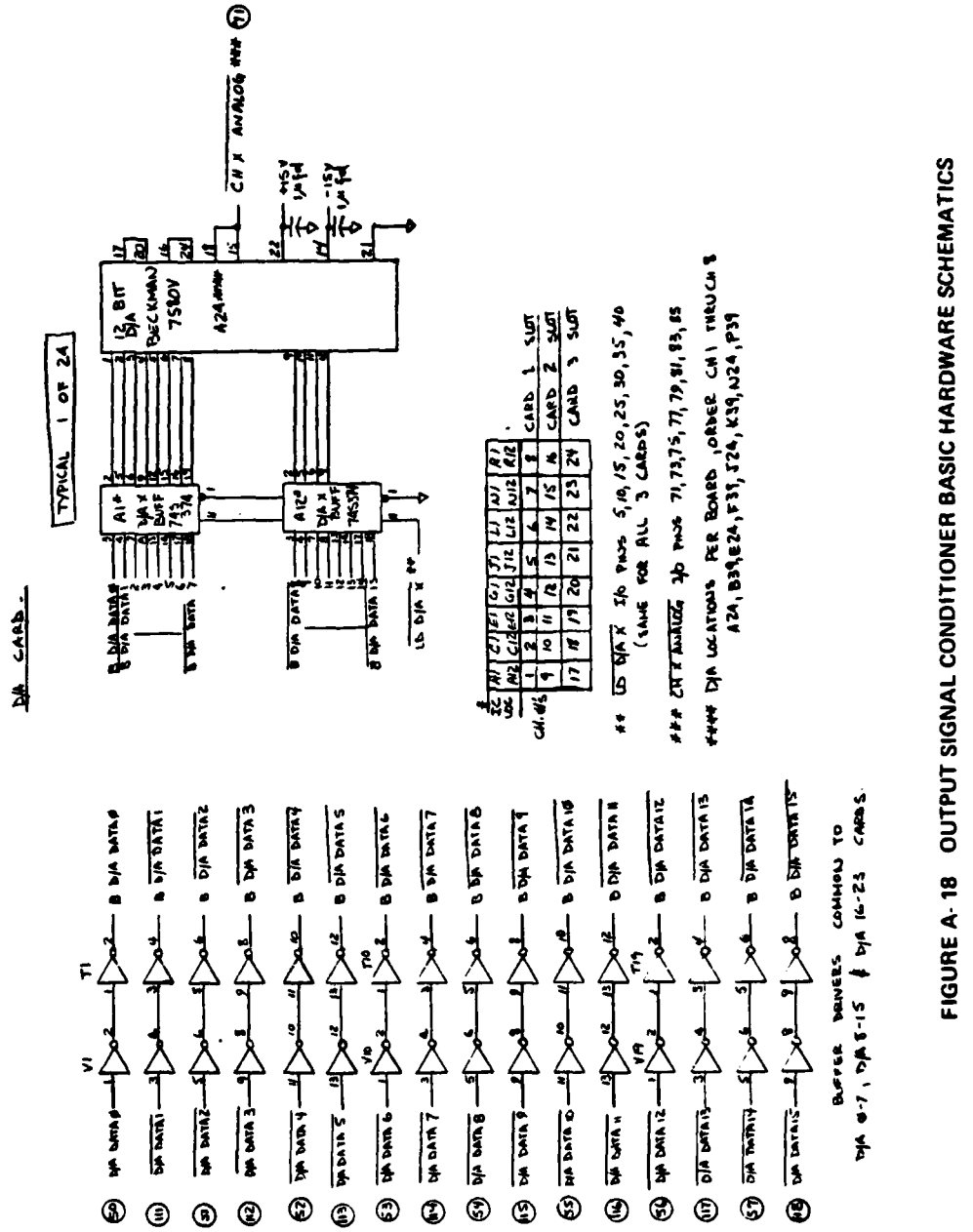


FIGURE A-18 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

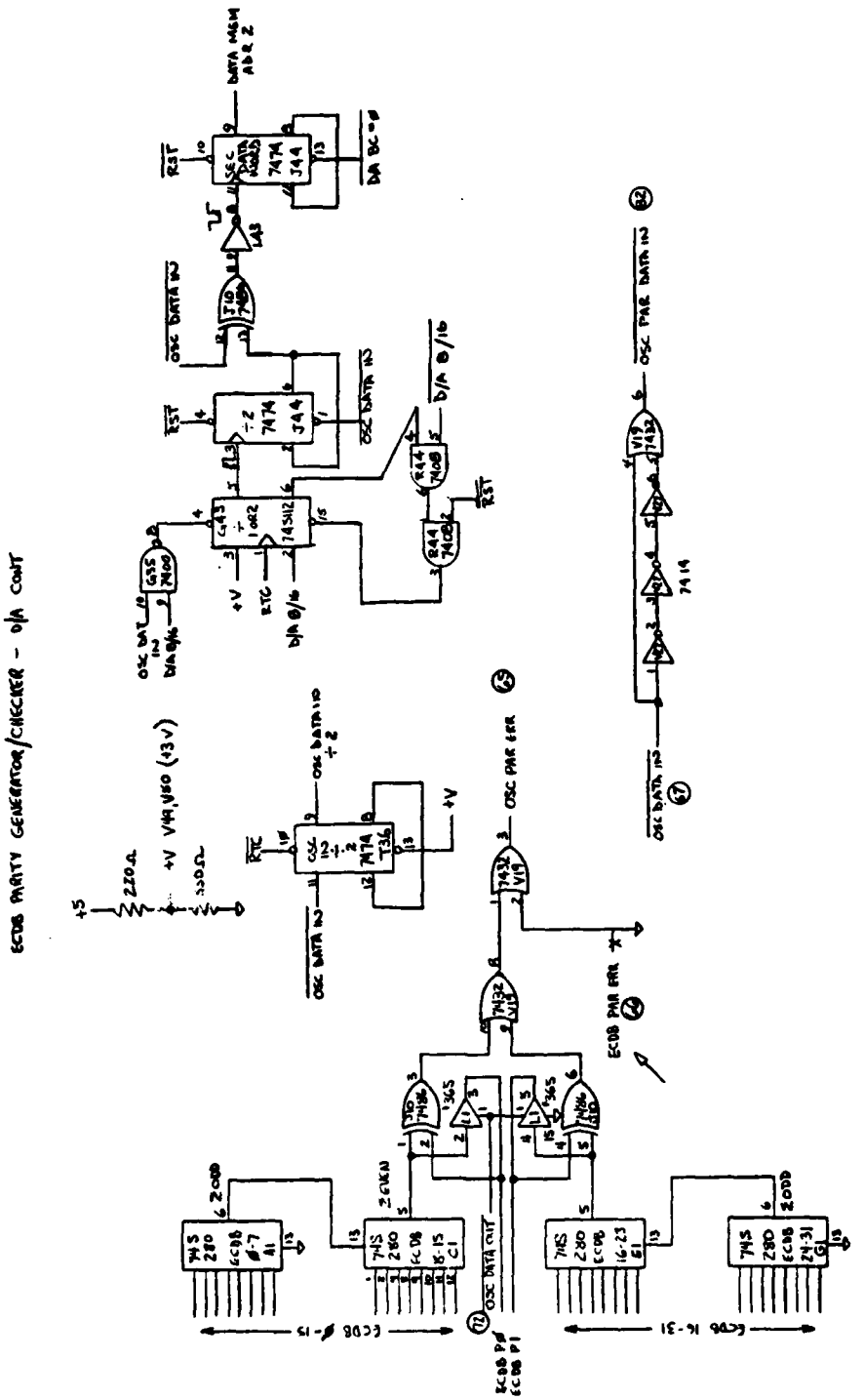


FIGURE A-19 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

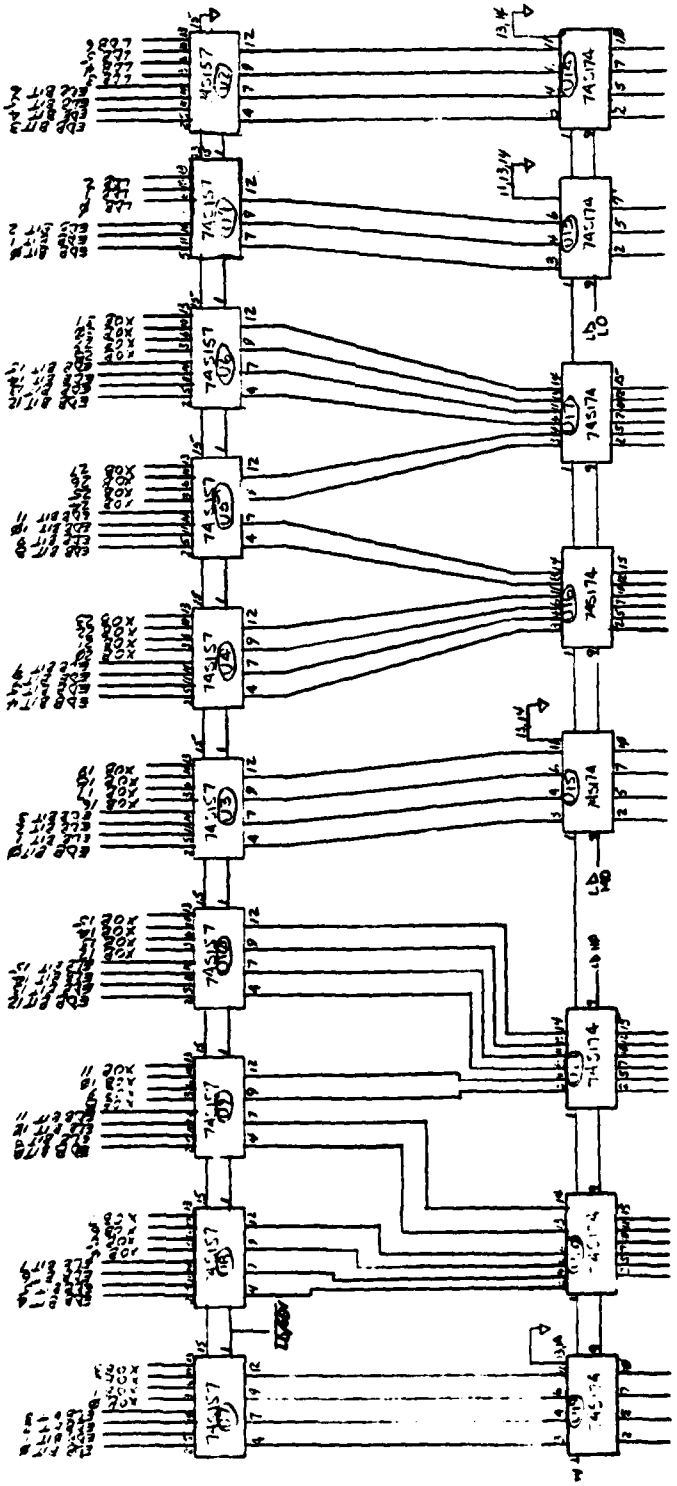
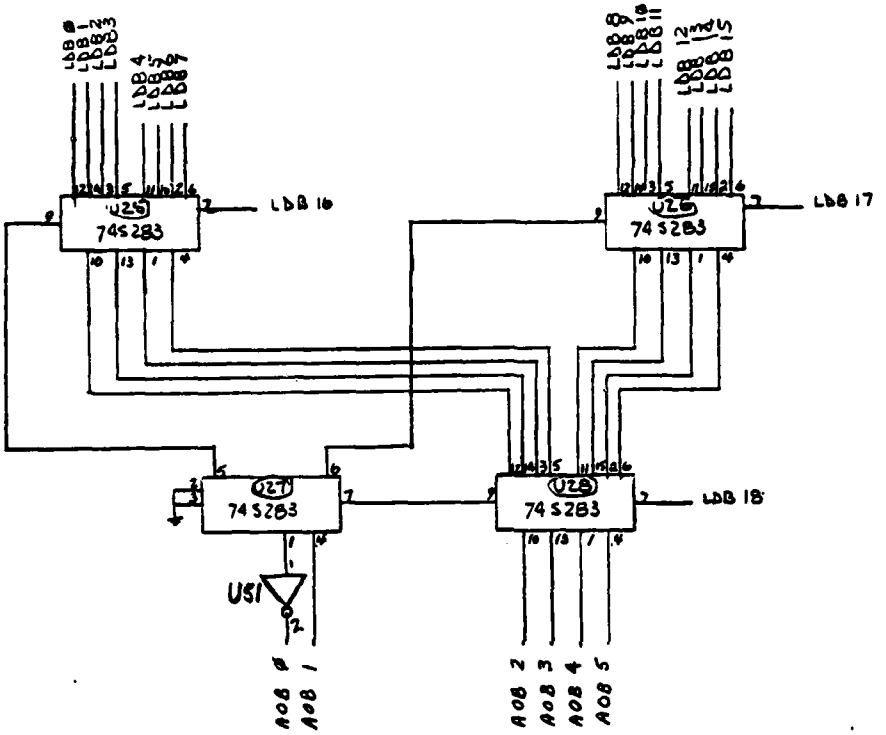


FIGURE A-20 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS



Rev Board 1
ADDER SCHEMATIC

FIGURE A-21 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

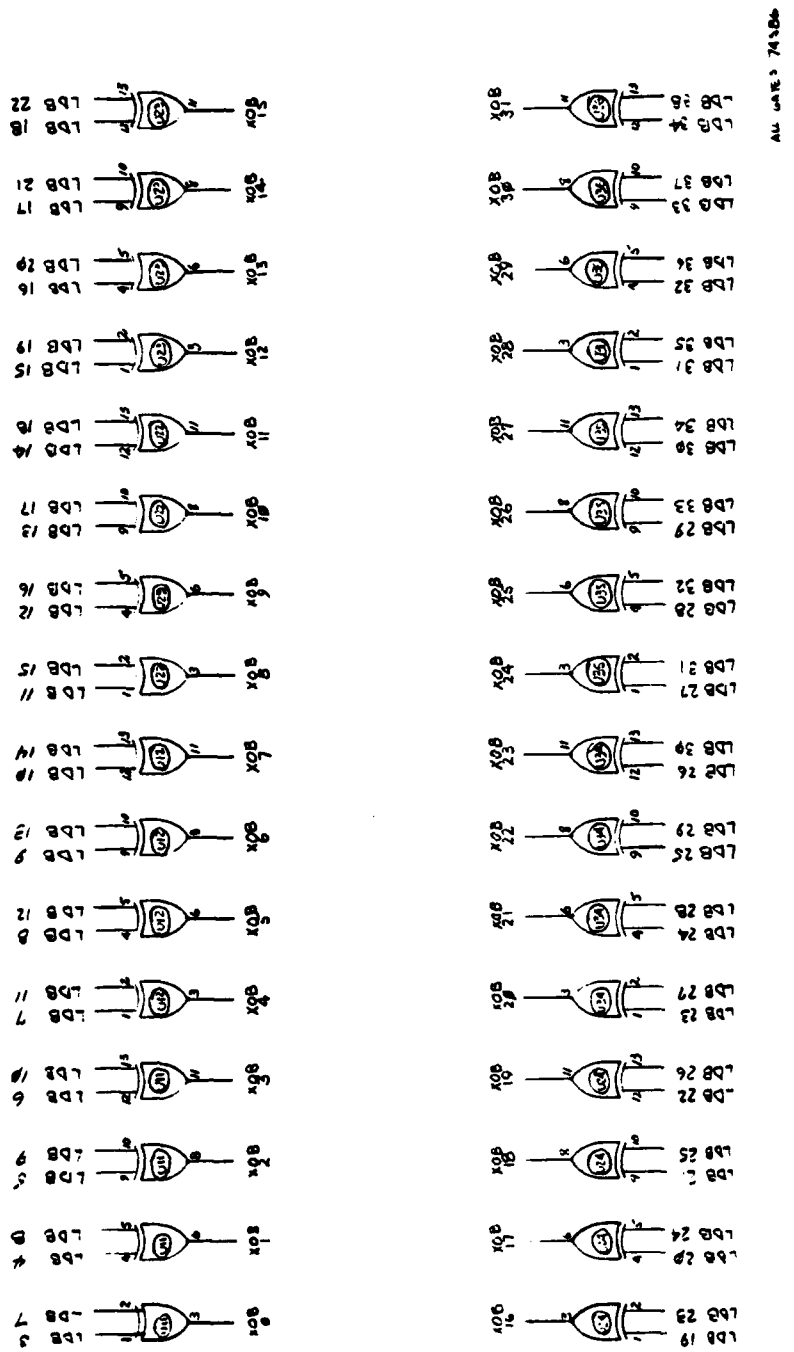


FIGURE A-22 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

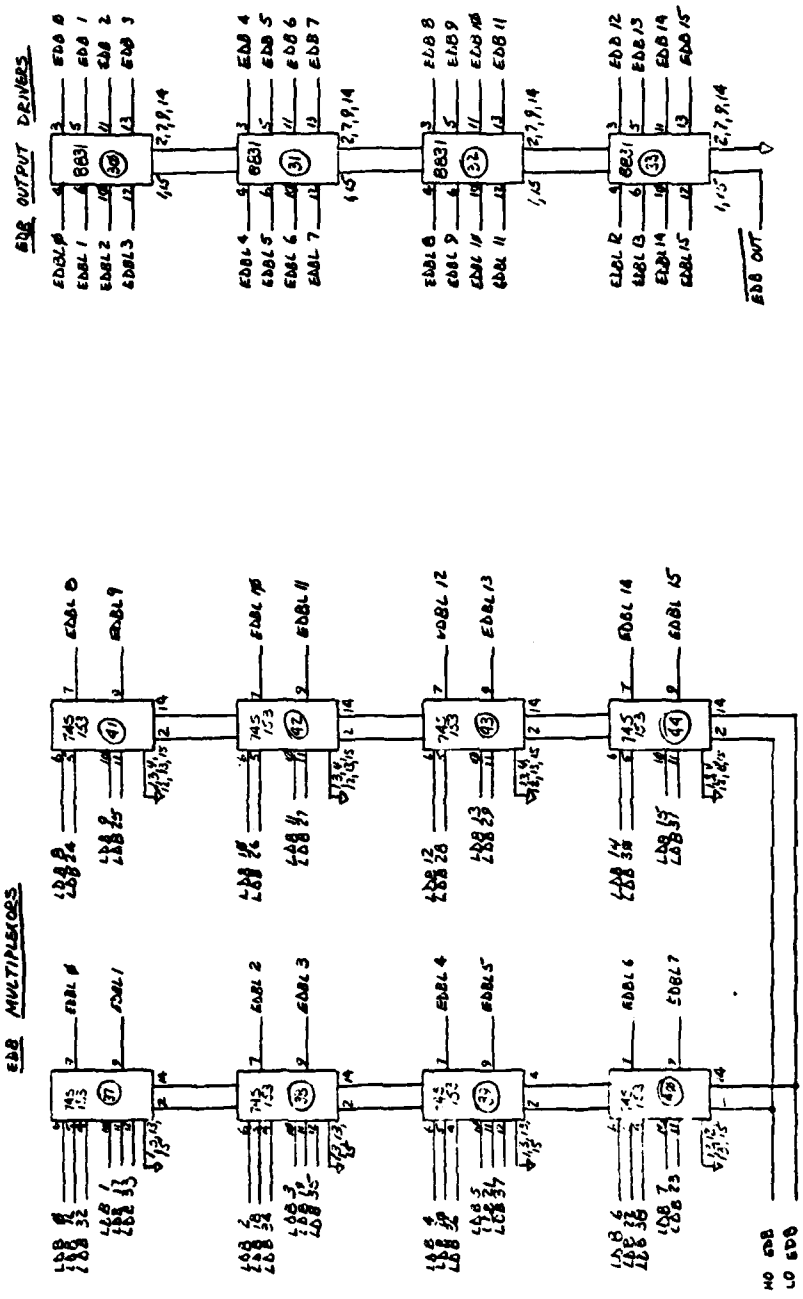


FIGURE A-23 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

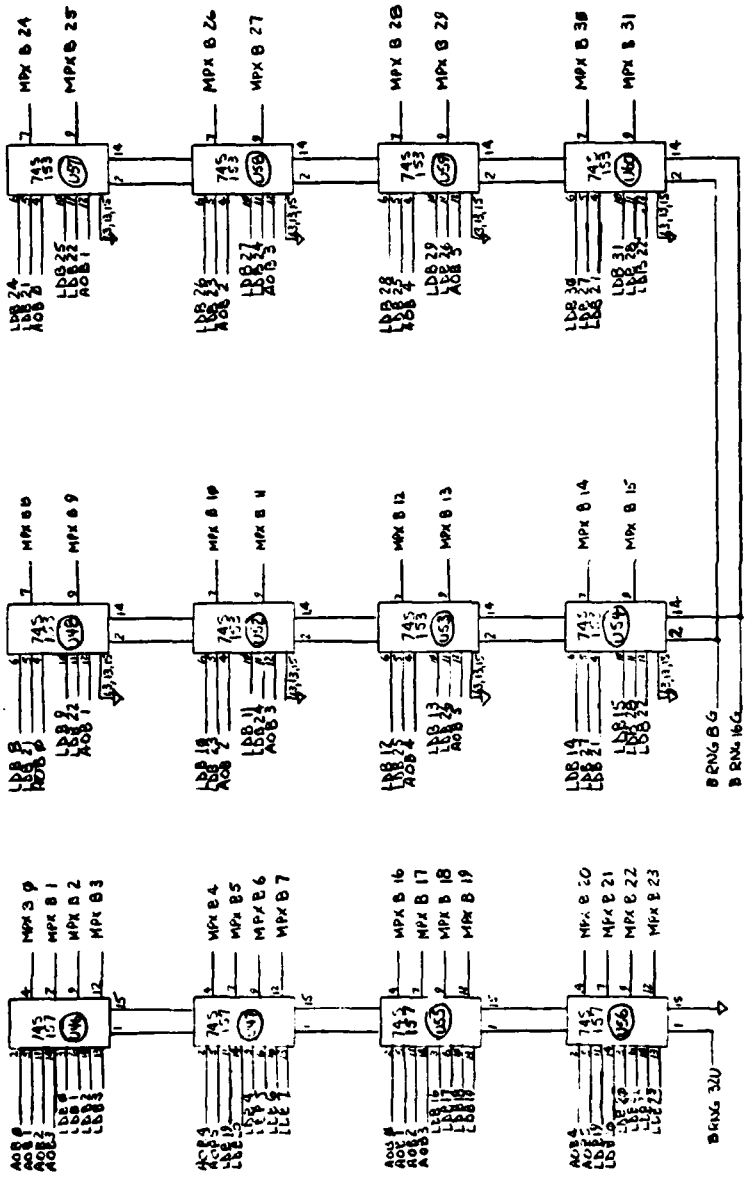


FIGURE A-24 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

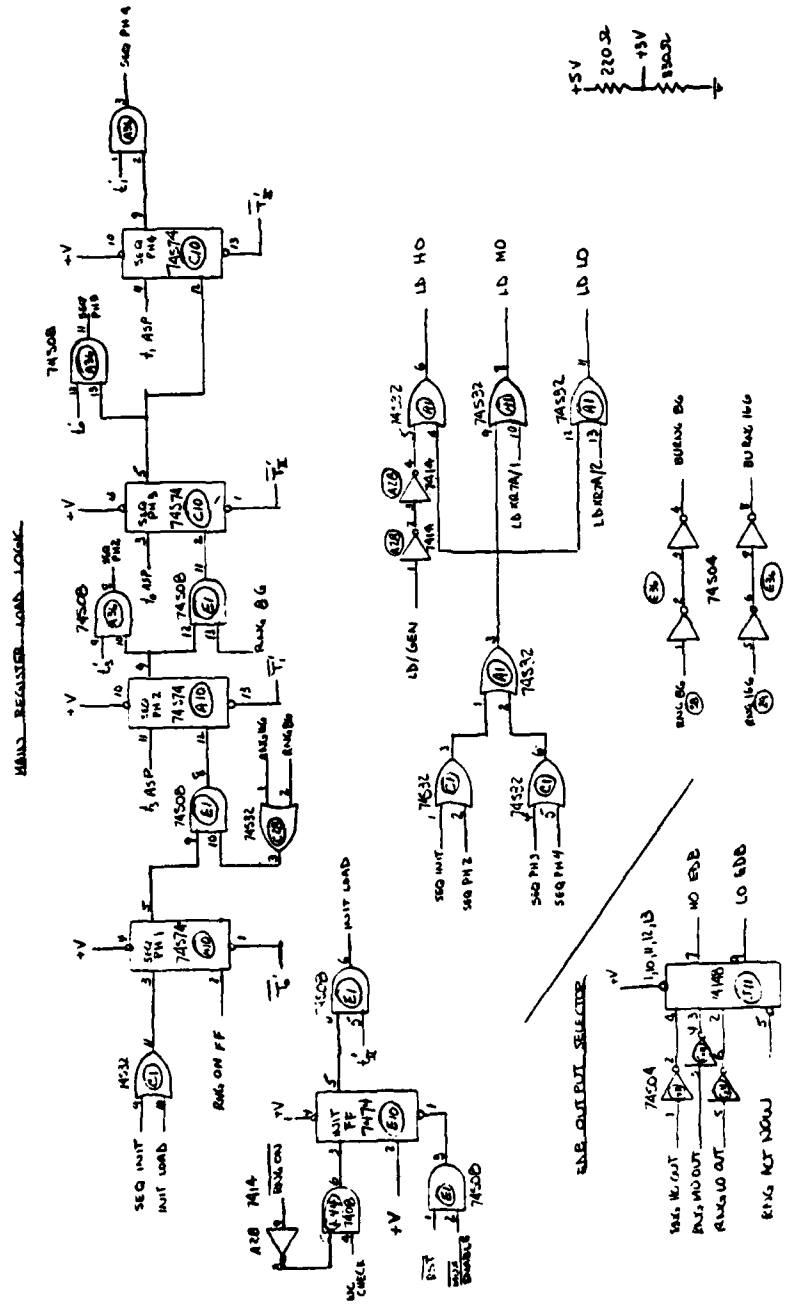


FIGURE A- 25 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

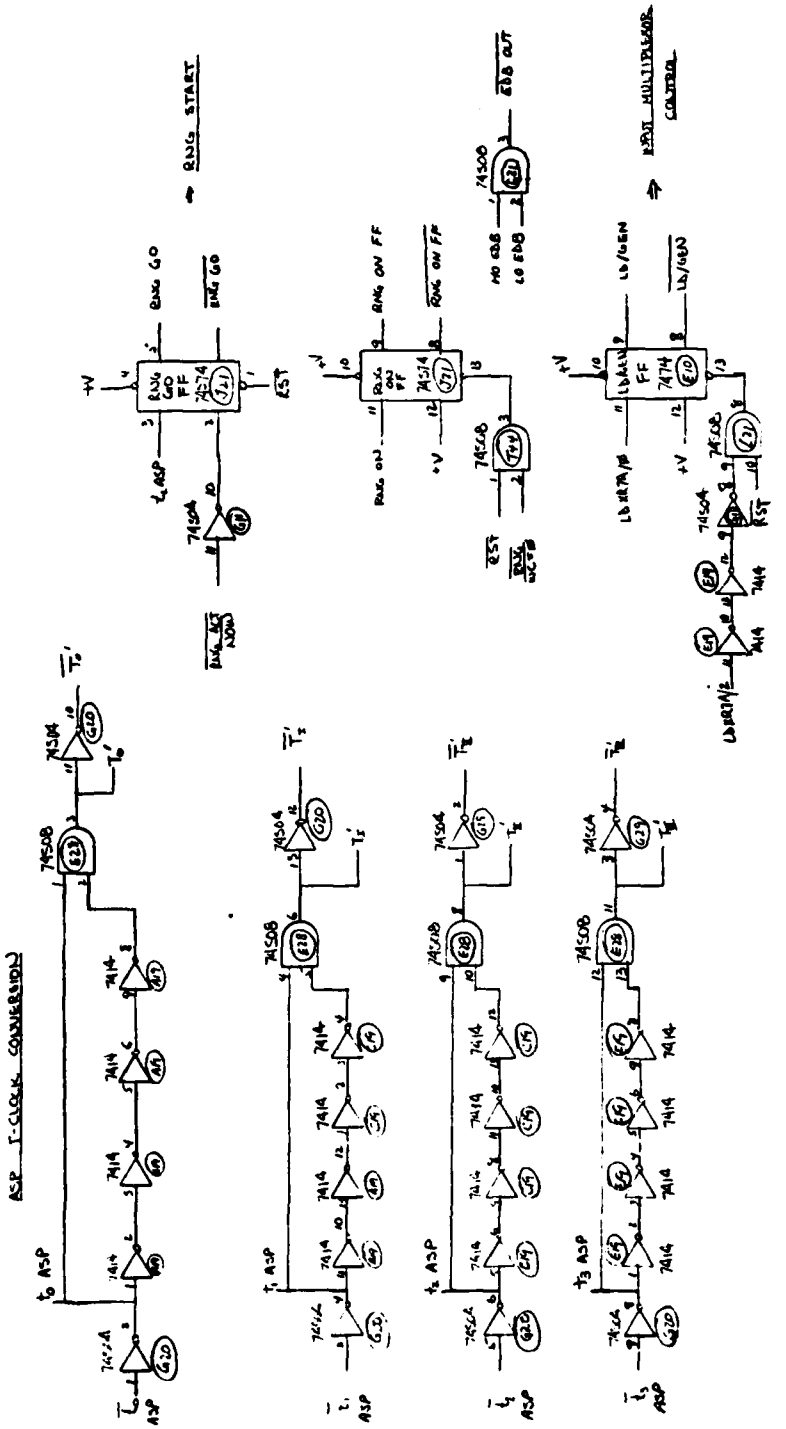


FIGURE A-26 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

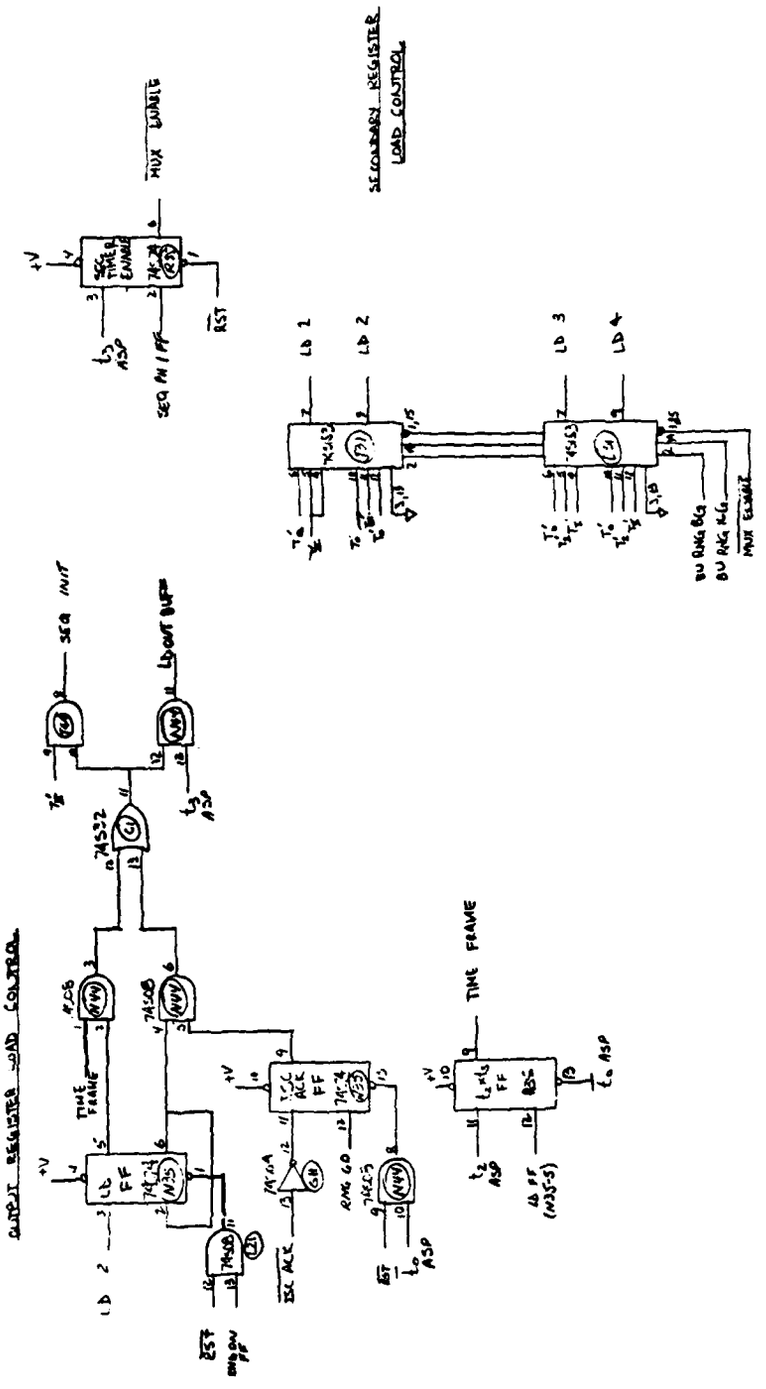


FIGURE A-27 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

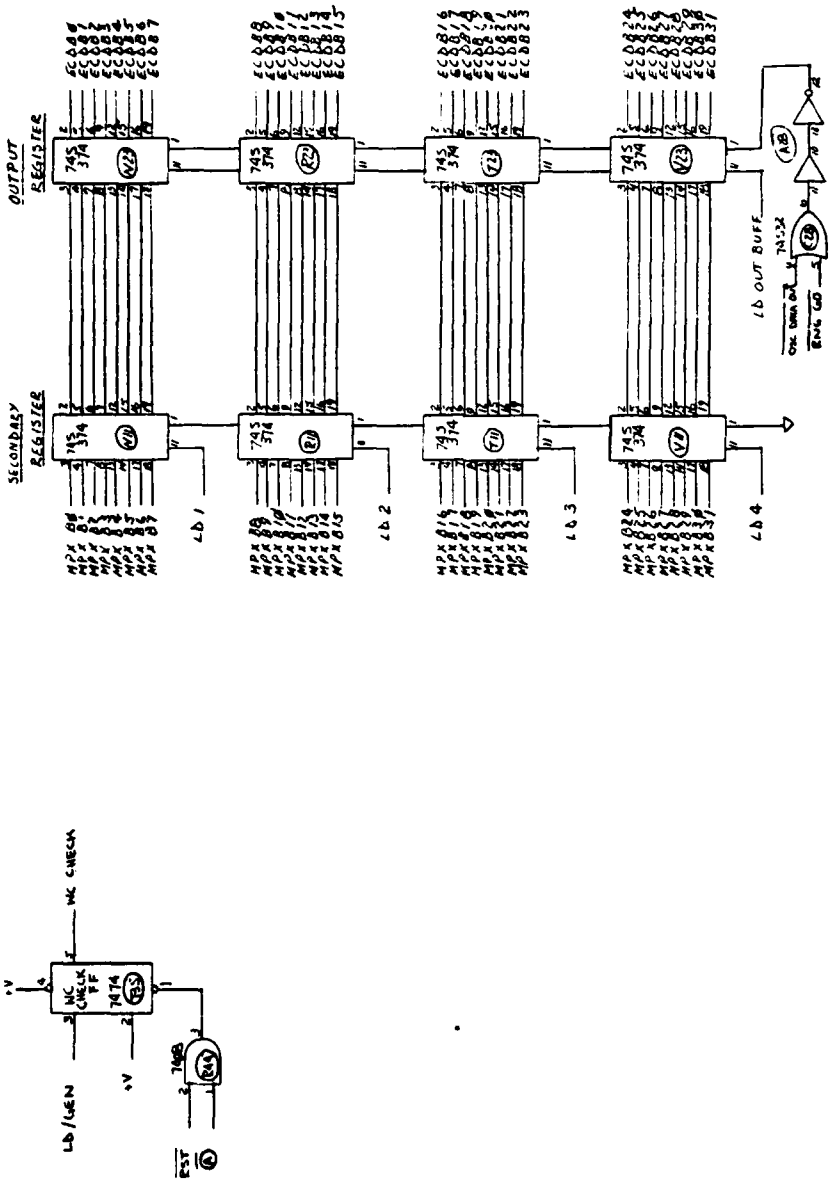


FIGURE A-28 OUTPUT SIGNAL CONDITIONER BASIC HARDWARE SCHEMATICS

APPENDIX B

CABLE INTERCONNECTION LISTS BETWEEN THE OUTPUT SIGNAL CONDITIONER BASIC HARDWARE AND THE AN/UYS-1

TABLE B-1 OSC CABLE 1 (J6/P6)

CONDUCTOR	P6* PIN	SIGNAL	BSAGC SLOT 17	DIP CONN	
1	49	G	–	G	MARK WITH BROWN STRIPE
2	8	ELDB R/W	88	8	
3	49	G	–	9	
4	91	BS REQ	89	7	
5	50**	G	–	10	
6	29	ILL BS ADR	90	6	
7	46	G	–	11	
8	25	DBL ECC ERR	91	5	
9	49	G	–	12	TIE ALL GNDS TOGETHER WITH ELBRI BUS AND TAKE 1 WIRE TO GND
10	70	ECDR PAP EPR	92	4	
11	–	G	–	13	
12	–	SPARE	93	3	
13	–	G	–	14	
14	–	SPARE	94	2	
15	60	G	–	15	
16	84	ISC ACK	95	1	
17	–	G	–	16	
18	44	TCLK0G	53	–	
19	65	TCLK0	50	–	
20	44	TCLK0G	53	–	
21	4	TCLK1G	53	–	
22	3	TCLK1	52	–	
23	4	TCLK1G	53	–	
24	24	TCLK2G	55	–	
25	45	TCLK2	54	–	
26	24	TCLK2G	55	–	
27	66	TCLK3G	55	–	
28	87	TCLK3	56	–	
29	66	TCLK3G	55	–	
30	60	G	–	G	
31	18	RD SEL 1	111	8	
32	–	G	–	9	
33	–	SPARE	112	7	
34	60	G	–	10	
35	39	RD SEL 2	113	6	
36	–	G	–	11	
37	–	SPARE	114	5	
38	60	G	–	12	TIE GNDS TOGETHER AS ABOVE
39	81	WRT SEL 1	115	4	
40	–	G	–	13	
41	–	SPARE	116	3	
42	60	G	–	14	
43	102	WRT SEL 2	117	2	
44	–	G	–	15	
45	–	SPARE	118	1	
46	–	G	–	16	
47	–	SPARE	–	–	
48	–	SPARE	–	–	
49	–	SPARE	–	–	
50	–	SPARE	–	–	

*GNDS NOT IN ORDER

**50 GETS SOME GNDS FROM CABLE 2
(WATCH FOR SIMILAR SITUATIONS)

TABLE B-2 OSC CABLE 2 J6/P6

COND.	P6 PIN	SIGNAL	D/A CONT SLOT 15	A/D CONT SLOT 7	RNG 3 SLOT 3	DIP CONN	
1	50	G	–	–	–	8	MARK WITH RED STRIPE
2	71	ECDB 0	10	3	3	9	
3	50	G	–	–	–	7	
4	92	ECDB 1	11	4	4	10	
5	50	G	–	–	–	6	
6	9	ECDB 2	12	5	5	11	
7	51	G	–	–	–	5	
8	30	ECDB 3	13	6	6	12	TIE GNDS TOGETHER AS BEFORE
9	51	G	–	–	–	4	
10	72	ECDB 4	14	7	7	13	
11	51	G	–	–	–	3	
12	93	ECDB 5	15	8	8	14	
13	51	G	–	–	–	2	
14	10	ECDB 6	16	9	9	15	
15	52	G	–	–	–	1	
16	31	ECDB 7	17	10	10	16	
17	52	G	–	–	–	8	
18	73	ECDB 8	19	12	12	9	
19	52	G	–	–	–	7	
20	94	ECDB 9	20	13	13	10	
21	52	G	–	–	–	6	
22	11	ECDB 10	21	14	14	11	
23	53	G	–	–	–	5	
24	32	ECDB 11	22	15	15	12	TIE GNDS TOGETHER
25	53	G	–	–	–	4	
26	74	ECDB 12	23	16	16	13	
27	53	G	–	–	–	3	
28	95	ECDB 13	24	17	17	14	
29	53	G	–	–	–	2	
30	12	ECDB 14	25	18	18	15	
31	54	G	–	–	–	1	
32	33	ECDB 15	26	19	19	16	
33	54	G	–	–	–	8	
34	75	ECDB 16	28	21	21	9	
35	54	G	–	–	–	7	
36	96	ECDB 17	29	22	22	10	
37	54	G	–	–	–	6	
38	13	ECDB 18	30	23	23	11	
39	55	G	–	–	–	5	
40	34	ECDB 19	31	24	24	12	TIE ALL GNDS TOGETHER
41	55	G	–	–	–	4	
42	76	ECDB 20	32	25	25	13	
43	55	5	–	–	–	3	
44	97	ECDB 21	33	26	26	14	
45	55	G	–	–	–	2	
46	–	SPARE	34	27	27	15	
47	–	G	–	–	–	1	
48	–	SPARE	35	28	28	16	
49	–	SPARE	–	–	–		
50	–	SPARE	–	–	–		

TABLE B-3 OSC CABLE 3 (J6/P6)

CONDUCTOR	P6 PIN	SIGNAL	D/A CONT SLOT 15	A/D CONT SLOT 7	RNG 2 SLOT 3	DIP CONN	
1	56	G	–	–	–	8	MARK WITH ORANGE STRIPE
2	14	ECDB 22	37	30	30	9	
3	56	G	–	–	–	7	
4	35	ECDB 23	38	31	31	10	
5	56	G	–	–	–	6	
6	77	ECDB 24	39	32	32	11	
7	56	G	–	–	–	5	
8	98	ECDB 25	40	33	33	12	TIE GNDS TOGETHER
9	56	G	–	–	–	4	
10	15	ECDB 26	41	34	34	13	
11	57	G	–	–	–	3	
12	36	ECDB 27	42	35	35	14	
13	57	G	–	–	–	2	
14	78	ECDB 28	43	36	36	15	
15	57	G	–	–	–	1	
16	99	ECDB 29	44	37	37	16	
17	57	G	–	–	–	8	
18	16	ECDB 30	46	39	39	9	
19	58	G	–	–	–	7	
20	37	ECDB 31	47	40	40	10	
21	58	G	–	–	–	6	
22	79	ECDB P1	48	41	41	11	
23	58	G	–	–	–	5	
24	19	ECDB P0	49	42	42	12	TIE GNDS TOGETHER
25	58	G	–		–	4	
26	–	SPARE	–		–	13	
27	–	G	–		–	3	
28	–	SPARE	–		–	14	
29	–	G	–		–	2	
30	–	SPARE	–		–	15	
31	–	G	–		–	1	
32	–	SPARE	–		–	16	
33-50	–	SPARE	–		–		

FOLD BACK AND TAPE

TABLE B-4 OSC CABLE 4 J6/P6

COND.	P6 PIN	SIGNAL	BSAG1 SLOT 21	DIP CONN	
1	46	G	–	G	MARK WITH
2	67	BS ADR 0	88	8	YELLOW STRIPE
3	46	G	–	9	
4	5	BS ADR 2	89	7	
5	47	G	–	10	
6	68	BS ADR 4	90	6	
7	47	G	–	11	
8	6	BS ADR 6	91	5	TIE GNDS
9	48	G	–	12	TOGETHER
10	69	BS ADR 8	92	4	
11	48	G	–	13	
12	7	BS ADR 10	93	3	
13	58	G	–	14	
14	100	BSM ADR 0	94	2	
15	59	G	–	15	
16	38	BSM ADR 2	95	1	
17	46	G	–	8	
18	88	BS ADR 1	27	9	
19	47	G	–	7	
20	26	BS ADR 3	28	10	
21	47	G	–	6	
22	89	BS ADR 5	29	11	
23	48	G	–	5	
24	27	BS ADR 7	30	12	TIE GNDS
25	48	G	–	4	TOGETHER
26	90	BS ADR 9	31	13	
27	49	G	–	3	
28	28	BS ADR 11	32	14	
29	59	G	–	2	
30	17	BSM ADR 1	33	15	
31	59	G	–	1	
32	80	BSM ADR 3	34	16	
33	59	G	36	–	
34	101	BSM ADR 4	96	–	
35	61	G	36	–	
36	40	BSM ADR 5	35	–	
37	2	G	36	–	
38-50	–	SPARE	–	–	

TABLE B-5 OSC CABLE 5 J9/P9 EDB BUS

CONDUCTOR	P9* PIN	SIGNAL	EDB/RTC SLOT 23	BSAG 1 SLOT 21	BSAG 2 SLOT 19	BSAGC SLOT 17	DIP CONN FOR SLOTS 7, 17, 19, 21, 23	RNG 1 SLOT 1	DIP CONN FOR SLOT 1
1	43	G	–	–	–	–	G	–	–
2	1	EDB 0	66	72	90	102	8	41	9
3	43	G	–	–	–	–	9	–	7
4	64	EDB 2	67	73	91	103	7	42	10
5	44	G	–	–	–	–	10	–	6
6	2	EDB 4	68	74	92	104	6	43	11
7	44	G	–	–	–	–	11	–	5
8	65	EDB 6	69	75	93	105	5	44	12
9	45	G	–	–	–	–	12	–	4
10	3	EDB 8	70	76	94	106	4	45	13
11	45	G	–	–	–	–	13	–	3
12	66	EDB 10	71	77	95	107	3	46	14
13	46	G	–	–	–	–	14	–	2
14	4	EDB 12	72	78	96	108	2	47	15
15	46	G	–	–	–	–	15	–	1
16	67	EDB 14	73	79	97	109	1	48	16
17	43	G	–	–	–	–	8	–	–
18	22	EDB 1	5	3	21	28	9	50	9
19	43	G	–	–	–	–	7	–	7
20	85	EDB 3	6	4	22	29	10	51	10
21	44	G	–	–	–	–	6	–	6
22	23	EDB 5	7	5	23	30	11	52	11
23	44	G	–	–	–	–	5	–	5
24	86	EDB 7	8	6	24	31	12	53	12
25	45	G	–	–	–	–	4	–	4
26	24	EDB 9	9	7	25	32	13	54	13
27	45	G	–	–	–	–	3	–	3
28	87	EDB 11	10	8	26	33	14	55	14
29	46	G	–	–	–	–	2	–	2
30	25	EDB 13	11	9	27	34	15	56	15
31	46	G	–	–	–	–	1	–	1
32	88	EDB 15	12	10	28	35	16	57	16
33	46	G	–	–	–	–	G	–	–
34	94	OSC INT	–	–	–	83	–	–	–
35	52	G	–	–	–	63	–	–	–
36-50	–	SPARE	–	–	–	–	–	–	–

TABLE B-6 OSC CABLE 6 – J9/P9

CONDUCTOR	P9 PIN	SIGNAL	EDB/RTC SLOT 23	DIP CONN	
1	47	G	–	G	MARK WITH
2	68	EAB 0	74	8	BLUE STRIPE
3	48	G	–	9	
4	6	EAB 2	75	7	
5	47	G	–	10	
6	89	EAB 1	76	6	
7	48	G	–	11	
8	27	EAB 3	77	5	TIE GNDS
9	50	G	–	12	TOGETHER
10	29	EB ACK	78	4	
11	47	G	–	13	
12	26	EDB P1	79	3	
13	50	G	–	14	
14	8	EDB SEC	80	2	
15	49	G	–	15	
16	91	EDB R/W	81	1	
17	48	G	–	8	
18	69	EAB 4	13	9	
19	49	G	–	7	
20	7	EAB 6	14	10	TIE GNDS
21	48	G	–	6	TOGETHER
22	90	EAB 5	15	11	
23	49	G	–	5	
24	28	EAB 7	16	12	
25	49	G	63	–	
26	70	EAB PAR	65	–	
27	50	G	63	–	
28	71	EB PAR ERR	64	–	
29	50	G	2	–	
30	92	SYS RST.	4	–	
31	52	G	2	–	
32	5	EDB P0	3	–	
33	52	G	2	–	
34-50	–	SPARE	–	–	

TABLE B-7 POWER CABLE INPUT POWER FOR OSC FROM AN/UYS-1

CONNECTOR	SIGNAL	
A1	+5V	RETURN
A2	+5V	
A3	+5V	RETURN
A4	+5V	
A5	+15V	
A6	±15V	RETURN
A7	−15V	

ALSO PIN 5 SHORTED TO PIN 6

APPENDIX C

OUTPUT SIGNAL CONDITIONER BASIC HARDWARE BACKPLANE WIRE LISTS

TABLE C-1 OSCBH BACK PLANE WIRING
(1 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD
A/D ACT NOW						80	40	64		
A/D BC = 0						70	15	109		
A/D WC = 0						5	7			
ARTC					69				31	
BS ADR MPX 15						39		38		
BS ADR OUT						38		84		
BSM ADR OUT						87		85		
D/A ACT NOW						57	38	66		
D/A BC = 0					6	86	13	108		
D/A BC = 0 DCL						9	67			
D/A DELFF						68	4			
D/A WC = 0						8	5			
D/A???16					71	101				
DEC RNG WD CTR						81	66	47		
EDB OUT	23	114								
HO EDB	20	111								
INIT 1						42	36			
IP1					68	64	70			
IP2						59	71			

TABLE C-1 OSCBH BACK PLANE WIRING
(2 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD
IP3						6	9			
LD A/D BS ADR CTR							3	99		
LD BS ADR REG						100		48		
LD D/A BS ADR CTR							65	98		
LD D/A 0				5	85					
LD D/A 1				10	86					
LD D/A 2				15	87					
LD D/A 3				20	88					
LD D/A 4				25	89					
LD D/A 5				30	90					
LD D/A 6				35	91					
LD D/A 7				40	92					
LD/GEN	25	113								
LD HO	18	108								
LD LO	16	110								
LD MO	17	109								
LDXR7A/0		56							22	
LDXR7A/1		57							24	
LDXR7A/2		59							26	
LDXR7A/3								20	23	

TABLE C-1 OSCBH BACK PLANE WIRING
(3 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD
LDXR7A/4								19	25	
LDXR7A15							100		27	
LDXR7C/0						120			88	
LDXR7C/1									28	
LDXR78/0								70	86	
LDXR78/1							120	80	82	
LDXR78/2							99		83	
LDXR78/3							37		85	
LDXR79/0								71	87	
LDXR79/1							59	81	89	
LDXR79/2							39		19	
LDXR79/3							98		21	
LO EDB	21	112								
MANUAL RST									30	
MPX ENCODER HO						82		59		
MPX ENCODER LO						84		120		
OSC DATA IN					67	72				
OSC DATA OUT		51			72	47				
OSC PAR ERR					65	26				
OSC RST IN						3			29	
RDXR7B/0						96			84	

TABLE C-1 OSCBH BACK PLANE WIRING
(4 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD
RNG ACT		50				78	101	65		
RNG HO OUT		11							17	
RNG LO OUT		85							20	
RNG MID OUT		76							18	
RNG WC = 0		117				7	11			
RNG 8B	28	38				110				
RNG 16G	29	29				49				
RNG 32U	30	20				51				
RST						67		67		
RST		54			70	65	68			
RTC					64				92	
RTC					8					
RTC ACT									91	
STATUS OUT									90	
0						66	87			
12.6 MHz					3	45			34	
12.6 MHz					4	46			35	

AD-A111 478 NAVAL SURFACE WEAPONS CENTER SILVER SPRING MD F/G 17/1
OUTPUT SIGNAL CONDITIONER BASIC HARDWARE.(U)
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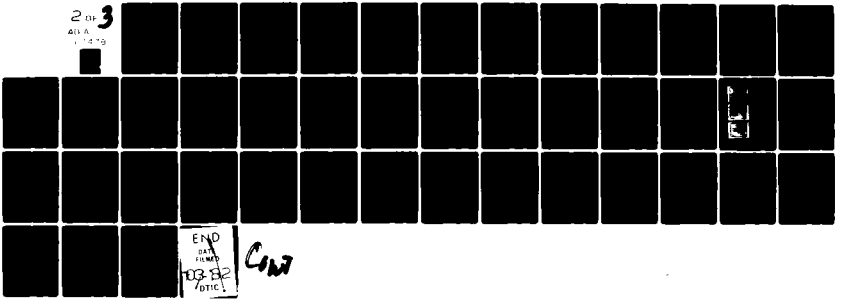

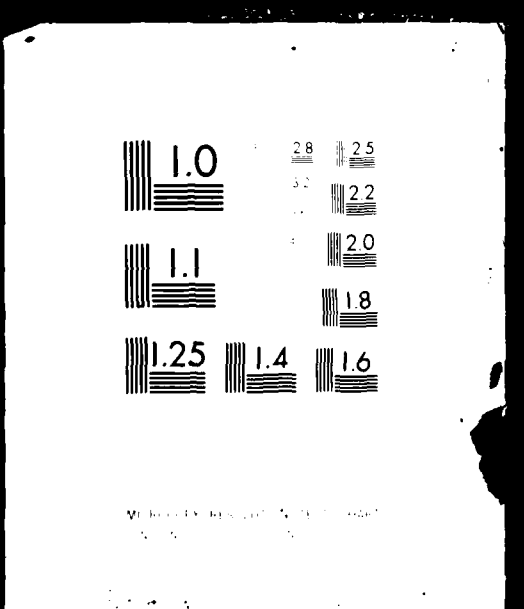

TABLE C-1 OSCBH BACK PLANE WIRING
(5 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD
RNG ACT		104				21				
EDP ACK										
PKE BUS						22			99	
RST XR 7B/0						23			100	
LD XR7A/1						24			101	
OSC DATA										
PAR IN					27	25				
PINGT INT	105	105	44		45	40	30	21	38	
LDXR7F	106	106	45		109	41	31	22	39	
SPARE 3	107	107	46		110	43	32	23	40	
SPARE 4	115	115	54		59	44	33	24	36	
SPARE 5	116	116	55		120	48	34	25	37	

TABLE C-1 OSCBH BACK PLANE WIRING
(6 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD
ECDB PAR ERR					66	92				
ISC ACK		103				95				
TCLK 0		45				50				
TCLK 1		47				52				
TCLK GND		46				53				
TCLK 2		43				54				
TCLK GND		48				55				
TCLK 3		49				56				
EDB ACK						36			78	
EDB SEL		53							80	
EDB R/W		52							81	

TABLE C-1 OSCBH BACK PLANE WIRING
(7 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD	DIP PINS
ADR ADDER 12							50	50			16
ADR ADDER 13							111	111			1
ADR ADDER 10							51	51			15
ADR ADDER 11							112	112			2
ADR ADDER 8							52	52			14
ADR ADDER 9							113	113			3
ADR ADDER 6							53	53			13
ADR ADDER 7							114	114			4
ADR ADDER 4							54	54			12
ADR ADDER 5							115	115			5
ADR ADDER 2							55	55			11
ADR ADDER 3							116	116			6
ADR ADDER 0							56	56			10
ADR ADDER 1							117	117			7
ADR ADDER 14							57	57			9
ADR ADDER 15							118	118			8

TABLE C-1 OSCBH BACK PLANE WIRING
(8 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD	DIP
BS ADR											
REG 1							41	39			16
REG 0							102	100			1
REG 3							42	40			15
REG 2							103	101			2
REG 5							43	41			14
REG 4							104	102			3
REG 7							44	42			13
REG 6							105	103			4
REG 9							45	43			12
REG 8							106	104			5
REG 11							46	44			11
REG 10							107	105			6
REG 13							47	45			10
REG 12							108	106			7
REG 15							48	46			9
BS ADR											
REG 14							109	107			8

TABLE C-1 OSCBH BACK PLANE WIRING
(9 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD	DIP
D/A BUFF CNT BUFF 0					73		73				16
CNT BUFF 1					74		74				15
CNT BUFF 2					75		75				14
CNT BUFF 3					76		76				13
CNT BUFF 4					77		77				12
CNT BUFF 5					78		78				11
CNT BUFF 6					79		79				10
D/A BUFF CNT BUFF 7					80		80				9

TABLE C-1 OSCBH BACK PLANE WIRING
(10 OF 12)

SIGNAL	D/A 16-23 SLOT 9	D/A 8-15 SLOT 11	D/A 0-7 SLOT 13	D/A CONT SLOT 15		DIP
D/A DATA 0	50	50	50	50		16
D/A DATA 1	111	111	111	111		1
D/A DATA 2	51	51	51	51		15
D/A DATA 3	112	112	112	112		2
D/A DATA 4	52	52	52	52		14
D/A DATA 5	113	113	113	113		3
D/A DATA 6	53	53	53	53		13
D/A DATA 7	114	114	114	114		4
D/A DATA 8	54	54	54	54		12
D/A DATA 9	115	115	115	115		5
D/A DATA 10	55	55	55	55		11
D/A DATA 11	116	116	116	116		6
D/A DATA 12	56	56	56	56		10
D/A DATA 13	117	117	117	117		7
D/A DATA 14	57	57	57	57		9
D/A DATA 15	118	118	118	118		8

TABLE C-1 OSCBH BACK PLANE WIRING
(11 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD	DIP PINS
MPXB 0	68	68									16
MPXB 1	69	69									15
MPXB 2	70	70									14
MPXB 3	71	71									13
MPXB 4	72	72									12
MPXB 5	73	73									11
MPXB 6	74	74									10
MPXB 7	75	75									9
MPXB 8	77	77									16
MPXB 9	78	78									15
MPXB 10	79	79									14
MPXB 11	80	80									13
MPXB 12	81	81									12
MPXB 13	82	82									11
MPXB 14	83	83									10
MPXB 15	84	84									9
MPXB 16	86	86									16
MPXB 17	87	87									15
MPXB 18	88	88									14
MPXB 19	89	89									13
MPXB 20	90	90									12

TABLE C-1 OSCBH BACK PLANE WIRING
(12 OF 12)

SIGNAL	RNG 1 SLOT 1	RNG 2 SLOT 3	A/D CONT SLOT 7	D/A 0-7 SLOT 13	D/A CONT SLOT 15	BSAGC SLOT 17	BSAG 2 SLOT 19	BSAG 1 SLOT 21	EDB/RTC SLOT 23	TEST BOARD	DIP PINS
MPXB 21	91	91									11
22	92	92									10
23	93	93									9
24	95	95									16
25	96	96									15
26	97	97									14
27	98	98									13
28	99	99									12
29	100	100									11
30	101	101									10
MPXB 31	102	102									9

TABLE C-2 BACKPLANE LOCATIONS OF D/A OUTPUT CHANNELS

SIGNAL	D/A 0-7 SLOT 13	D/A 8-15 SLOT 11	D/A 14-23 SLOT 9
CH 0	71		
CH 1	73		
CH 2	75		
CH 3	77		
CH 4	79		
CH 5	81		
CH 6	83		
CH 7	85		
CH 8		71	
CH 9		73	
CH 10		75	
CH 11		77	
CH 12		79	
CH 13		81	
CH 14		83	
CH 15		85	
CH 16			71
CH 17			73
CH 18			75
CH 19			77
CH 20			79
CH 21			81
CH 22			83
CH 23			85

TABLE C-3 DISCRETE WIRING

SIGNAL	D/A 16-23 SLOT 9	D/A 8-15 SLOT 11	D/A 0-7 SLOT 13	D/A CONT SLOT 15
LD D/A 8		5		93
LD D/A 9		10		94
LD D/A 10		15		95
LD D/A 11		20		96
LD D/A 12		25		97
LD D/A 13		30		98
LD D/A 14		35		99
LD D/A 15		40		100
LD D/A 16	5			101
LD D/A 17	10			102
LD D/A 18	15			103
LD D/A 19	20			104
LD D/A 20	25			105
LD D/A 21	30			106
LD D/A 22	35			107
LD D/A 23	40			108
+15 V	66	66	66	
−15 V	69	69	69	
GND	70	70	70	

TABLE C-4 CONTROL BUS EDB/RTC SLOT 23

SIGNAL	EDB/RTC SLOT 23	DIP PIN	CABLE CONDUCTORS
CB 0	41	16	1
CB 1	102	1	2
CB 2	42	15	3
CB 3	103	2	4
CB 4	43	14	5
CB 5	104	3	6
CB 6	44	13	7
CB 7	105	4	8
CB 8	45	12	9
CB 9	106	5	10
CB 10	46	11	11
CB 11	107	6	12
CB 12	47	10	13
CB 13	108	7	14
CB 14	48	9	15
CB 15	109	8	16
CB 16	50	16	17
CB 17	111	1	18
CB 18	51	15	19
CB 19	112	2	20
CB 20	52	14	21
CB 21	113	3	22
CB 22	53	13	23
CB 23	114	4	24
CB 24	54	12	25
CB 25	115	5	26
CB 26	55	11	27
CB 27	116	6	28
CB 28	56	10	29
CB 29	117	7	30
CB 30	57	9	31
CB 31	118	8	32
SPARE			33-50

APPENDIX D

OSCBH CIRCUIT BOARD INPUT/OUTPUT PIN ASSIGNMENTS

TABLE D-1 RNG 1 BOARD SLOT 1

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41	EDB 0	102	MPXB 31
2	GND	63	GND	42	EDB 2	103	
3		64		43	EDB 4	104	
4		65		44	EDB 6	105	
5		66		45	EDB 8	106	
6		67		46	EDB 10	107	
7		68	MPXB 0	47	EDB 12	108	
8		69	MPXB 1	48	EDB 14	109	
9		70	MPXB 2	49		110	
10		71	MPXB 3	50	EDB 1	111	
11		72	MPXB 4	51	EDB 3	112	
12		73	MPXB 5	52	EDB 5	113	
13		74	MPXB 6	53	EDB 7	114	
14		75	MPXB 7	54	EDB 9	115	
15		76		55	EDB 11	116	
16	LD LO	77	MPXB 8	56	EDB 13	117	
17	LD MO	78	MPXB 9	57	EDB 15	118	
18	LD HO	79	MPXB 10	58	(KEY)	119	(KEY)
19		80	MPXB 11	59		120	
20	HO EDB	81	MPXB 12	60	+5V	121	+5V
21	LO EDB	82	MPXB 13	61	+5V	122	+5V
22		83	MPXB 14				
23	EDB OUT	84	MPXB 15				
24		85					
25	LD/GEN	86	MPXB 16				
26		87	MPXB 17				
27		88	MPXB 18				
28	RNG 8G	89	MPXB 19				
29	RNG 16G	90	MPXB 20				
30	RNG 32U	91	MPXB 21				
31		92	MPXB 22				
32		93	MPXB 23				
33		94					
34		95	MPXB 24				
35		96	MPXB 25				
36		97	MPXB 26				
37		98	MPXB 27				
38		99	MPXB 28				
39		100	MPXB 29				
40		101	MPXB 30				

TABLE D-2 RNG 2 BOARD SLOT 3

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41	ECDB P1	102	MPXB 31
2	GND	63	GND	42	ECDB P0	103	ISC ACK
3	ECDB 0	64		43	TCLK 2	104	RNG ACT
4	ECDB 1	65		44		105	SPARE 1
5	ECDB 2	66		45	TCLK 0	106	SPARE 2
6	ECDB 3	67		46	TCLK GND	107	SPARE 3
7	ECDB 4	68	MPXB 0	47	TCLK 1	108	LD HO
8	ECDB 5	69	MPXB 1	48	TCLK GND	109	LD MO
9	ECDB 6	70	MPXB 2	49	TCLK 3	110	LD LO
10	ECDB 7	71	MPXB 3	50	RNG ACT NOW	111	HO EDB
11	RNG HO OUT	72	MPXB 4	51	OSC DATA OUT	112	LO EDB
12	ECDB 8	73	MPXB 5	52	EDB R/W	113	LD/GEN
13	ECDB 9	74	MPXB 6	53	EDB SEL	114	EDB OUT
14	ECDB 10	75	MPXB 7	54	RST	115	SPARE 4
15	ECDB 11	76	RNG MO OUT	55		116	SPARE 5
16	ECDB 12	77	MPXB 8	56	LDXR7A/0	117	RNG WC = 0
17	ECDB 13	78	MPXB 9	57	LDXR7A/1	118	
18	ECDB 14	79	MPXB 10	58	(KEY)	119	(KEY)
19	ECDB 15	80	MPXB 11	59	LDXR7A/2	120	
20	RNG 32U	81	MPXB 12	60	+5V	121	+5V
21	ECDB 16	82	MPXB 13	61	+5V	122	+5V
22	ECDB 17	83	MPXB 14				
23	ECDB 18	84	MPXB 15				
24	ECDB 19	85	RNG LO OUT				
25	ECDB 20	86	MPXB 16				
26	ECDB 21	87	MPXB 17				
27	SPARE	88	MPXB 18				
28	SPARE	89	MPXB 19				
29	RNG 16G	90	MPXB 20				
30	ECDB 22	91	MPXB 21				
31	ECDB 23	92	MPXB 22				
32	ECDB 24	93	MPXB 23				
33	ECDB 25	94					
34	ECDB 26	95	MPXB 24				
35	ECDB 27	96	MPXB 25				
36	ECDB 28	97	MPXB 26				
37	ECDB 29	98	MPXB 27				
38	RNG 8G	99	MPXB 28				
39	ECDB 30	100	MPXB 29				
40	ECDB 31	101	MPXB 30				

TABLE D-3 A/D CONT SLOT 7

PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND
2	GND	63	GND
3	ECDB 0	64	
4	ECDB 1	65	
5	ECDB 2	66	
6	ECDB 3	67	
7	ECDB 4	68	
8	ECDB 5	69	
9	ECDB 6	70	
10	ECDB 7	71	
11		72	
12	ECDB 8	73	
13	ECDB 9	74	
14	ECDB 10	75	
15	ECDB 11	76	
16	ECDB 12	77	
17	ECDB 13	78	
18	ECDB 14	79	
19	ECDB 15	80	
20		81	
21	ECDB 16	82	
22	ECDB 17	83	
23	ECDB 18	84	
24	ECDB 19	85	
25	ECDB 20	86	
26	ECDB 21	87	
27	SPARE	88	
28	SPARE	89	
29		90	
30	ECDB 22	91	
31	ECDB 23	92	
32	ECDB 24	93	
33	ECDB 25	94	
34	ECDB 26	95	
35	ECDB 27	96	
36	ECDB 28	97	
37	ECDB 29	98	
38		99	
39	ECDB 30	100	
40	ECDB 31	101	

PIN	SIGNAL	PIN	SIGNAL
41	ECDB P1	102	EDB 0
42	ECDB P0	103	EDB 2
43		104	EDB 4
44	SPARE 1	105	EDB 6
45	SPARE 2	106	EDB 8
46	SPARE 3	107	EDB 10
47		108	EDB 12
48		109	EDB 14
49		110	
50		111	EDB 1
51		112	EDB 3
52		113	EDB 5
53		114	EDB 7
54	SPARE 4	115	EDB 9
55	SPARE 5	116	EDB 11
56		117	EDB 13
57		118	EDB 15
58	(KEY)	119	(KEY)
59		120	
60	+5V	121	+5V
61	+5V	122	+5V

TABLE D-4 D/A 16-23 SLOT 9

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41		102	
2	GND	63	GND	42		103	
3		64		43		104	
4		65		44		105	
5	LD D/A 16	66	+15V	45		106	
6		67		46		107	
7		68		47		108	
8		69	−15V	48		109	
9		70	GND	49		110	
10	LD D/A 17	71	CH 16	50	D/A DATA 0	111	D/A DATA 1
11		72	CH 16 GND	51	D/A DATA 2	112	D/A DATA 3
12		73	CH 17	52	D/A DATA 4	113	D/A DATA 5
13		74	CH 17 GND	53	D/A DATA 6	114	D/A DATA 7
14		75	CH 18	54	D/A DATA 8	115	D/A DATA 9
15	LD D/A 18	76	CH 18 GND	55	D/A DATA 10	116	D/A DATA 11
16		77	CH 19	56	D/A DATA 12	117	D/A DATA 13
17		78	CH 19 GND	57	D/A DATA 14	118	D/A DATA 15
18		79	CH 20	58	(KEY)	119	(KEY)
19		80	CH 20 GND	59		120	
20	LD D/A 19	81	CH 21	60	+5V	121	+5V
21		82	CH 21 GND	61	+5V	122	+5V
22		83	CH 22				
23		84	CH 22 GND				
24		85	CH 23				
25	LD D/A 20	86	CH 23 GND				
26		87					
27		88					
28		89					
29		90					
30	LD D/A 21	91					
31		92					
32		93					
33		94					
34		95					
35	LD D/A 22	96					
36		97					
37		98					
38		99					
39		100					
40	LD D/A 23	101					

TABLE D-5 D/A 8-15 SLOT 11

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41		102	
2	GND	63	GND	42		103	
3		64		43		104	
4		65		44		105	
5	LD D/A 8	66	+15V	45		106	
6		67		46		107	
7		68		47		108	
8		69	-15V	48		109	
9		70	GND	49		110	
10	LD D/A 9	71	CH 8	50	D/A DATA 0	111	D/A DATA 1
11		72	CH 18 GND	51	D/A DATA 2	112	D/A DATA 3
12		73	CH 9	52	D/A DATA 4	113	D/A DATA 5
13		74	CH 9 GND	53	D/A DATA 6	114	D/A DATA 7
14		75	CH 10	54	D/A DATA 8	115	D/A DATA 9
15	LD D/A 10	76	CH 10 GND	55	D/A DATA 10	116	D/A DATA 11
16		77	CH 11	56	D/A DATA 12	117	D/A DATA 13
17		78	CH 11 GND	57	D/A DATA 14	118	D/A DATA 15
18		79	CH 12	58	(KEY)	119	(KEY)
19		80	CH 12 GND	59		120	
20	LD D/A 19	81	CH 13	60	+5V	121	+5V
21		82	CH 13 GND	61	+5V	122	+5V
22		83	CH 14				
23		84	CH 14 GND				
24		85	CH 15				
25	LD D/A 12	86	CH 15 GND				
26		87					
27		88					
28		89					
29		90					
30	LD D/A 13	91					
31		92					
32		93					
33		94					
34		95					
35	LD D/A 14	96					
36		97					
37		98					
38		99					
39		100					
40	LD D/A 15	101					

TABLE D-6 D/A 0-7 SLOT 13

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41		102	
2	GND	63	GND	42		103	
3		64		43		104	
4		65		44		105	
5	LD D/A 0	66	+15V	45		106	
6		67		46		107	
7		68		47		108	
8		69	−15V	48		109	
9		70	GND	49		110	
10	LD D/A 1	71	CH 0	50	D/A DATA 0	111	D/A DATA 1
11		72	CH 0 GND	51	D/A DATA 2	112	D/A DATA 3
12		73	CH 1	52	D/A DATA 4	113	D/A DATA 5
13		74	CH 1 GND	53	D/A DATA 6	114	D/A DATA 7
14		75	CH 2	54	D/A DATA 8	115	D/A DATA 9
15	LD D/A 2	76	CH 2 GND	55	D/A DATA 10	116	D/A DATA 11
16		77	CH 3	56	D/A DATA 12	117	D/A DATA 13
17		78	CH 3 GND	57	D/A DATA 14	118	D/A DATA 15
18		79	CH 4	58	(KEY)	119	(KEY)
19		80	CH 4 GND	59		120	
20	LD D/A 3	81	CH 5	60	+5V	121	+5V
21		82	CH 5 GND	61	+5V	122	+5V
22		83	CH 6				
23		84	CH 6 GND				
24		85	CH 7				
25	LD D/A 4	86	CH 7 GND				
26		87					
27		88					
28		89					
29		90					
30	LD D/A 5	91					
31		92					
32		93					
33		94					
34		95					
35		96					
36	LD D/A 6	97					
37		98					
38		99					
39		100					
40	LD D/A 7	101					

TABLE D-7 D/A CONT SLOT 15

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41	ECDB 26	102	LD D/A 17
2	GND	63	GND	42	ECDB 27	103	LD D/A 18
3	12.6 MHz	64	RTC	43	ECDB 28	104	LD D/A 19
4	12.6 MHz GND	65	OSC PAR ERR	44	ECDB 29	105	LD D/A 20
5		66	ECDB PAR ERR	45	SPARE 1	106	LD D/A 21
6	D/A BC = 0	67	OSC DATA IN	46	ECDB 30	107	LD D/A 22
7		68	IP1	47	ECDB 31	108	LD D/A 23
8	RTC	69	ARTC	48	ECDB P1	109	SPARE 2
9		70	RST	49	ECDB P0	110	SPARE 3
10	ECDB 0	71	D/A 8/16	50	D/A DATA 0	111	D/A DATA 1
11	ECDB 1	72	OSC DATA OUT	51	D/A DATA 2	112	D/A DATA 3
			D/A BUFF				
12	ECDB 2	73	CNT BUFF 0	52	D/A DATA 4	113	D/A DATA 5
13	ECDB 3	74	1	53	D/A DATA 6	114	D/A DATA 7
14	ECDB 4	75	2	54	D/A DATA 8	115	D/A DATA 9
15	ECDB 5	76	3	55	D/A DATA 10	116	D/A DATA 11
16	ECDB 6	77	4	56	D/A DATA 12	117	D/A DATA 13
17	ECDB 7	78	5	57	D/A DATA 14	118	D/A DATA 15
18		79	6	58	(KEY)	119	(KEY)
			D/A BUFF				
19	ECDB 8	80	CNT BUFF 7	59	SPARE 4	120	SPARE 5
20	ECDB 9	81		60	+5V	121	+5V
21	ECDB 10	82		61	+5V	122	+5V
22	ECDB 11	83					
23	ECDB 12	84					
24	ECDB 13	85	LD D/A 0				
25	ECDB 14	86	LD D/A 1				
26	ECDB 15	87	LD D/A 2				
	OSC DATA						
27	PAR IN	88	LD D/A 3				
28	ECDB 16	89	LD D/A 4				
29	ECDB 17	90	LD D/A 5				
30	ECDB 18	91	LD D/A 6				
31	ECDB 19	92	LD D/A 7				
32	ECDB 20	93	LD D/A 8				
33	ECDB 21	94	LD D/A 9				
34	SPARE	95	LD D/A 10				
35	SPARE	96	LD D/A 11				
36		97	LD D/A 12				
37	ECDB 22	98	LD D/A 13				
38	ECDB 23	99	LD D/A 14				
39	ECDB 24	100	LD D/A 15				
40	ECDB 25	101	LD D/A 16				

TABLE D-8 BSAGC SLOT 17

PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND
2	GND	63	GND
3	OSC RST IN	64	IP 1
4	RTC	65	RST
5	A/D WC = 0	66	0
6	IP 3	67	RST
7	RNG WC = 0	68	D/A DEL FF
8	D/A WC = 0	69	
9	D/A BC = 0	70	A/D BC = 0
10	DEL	71	
11		72	OSC DATA IN
12		73	
13		74	
14		75	
15		76	
16		77	
17		78	RNG ACT NOW
18		79	
19		80	A/D ACT NOW
20		81	DEC RNG WD CTR MPX
21	RNG ACT EDB ACK	82	ENCODER HO
22	PRE BUS	83	OSC INT MPX
23	RST XR7B/0	84	ENCODER LO
24	LDXR7A/1 OSC DATA	85	
25	PAR IN	86	D/A BC = 0
26	OSC PAR ERR	87	BSM ADR OUT
27		88	ECDB R/W
28	EDB 1	89	BS REQ
29	EDB 3	90	ILL BS ADR
30	EDB 5	91	DBL ECC ERR
31	EDB 7	92	ECDB PAR ERR
32	EDB 9	93	
33	EDB 11	94	
34	EDB 13	95	ISC ACK
35	EDB 15	96	RDXR7B/0
36	EDB ACK	97	
37		98	
38	BS ADR OUT	99	
39	BS ADR MPX15	100	LD BS ADR REG
40	SPARE 1	101	D/A 8/16
41	SPARE 2	102	EDB 0
42	INIT 1	103	EDB 2
43	SPARE 3	104	EDB 4
44	SPARE 4	105	EDB 6
45	12.6 MHz	106	EDB 8
46	12.6 MHz GND	107	EDB 10
47	OSC DATA OUT	108	EDB 12
48	SPARE 5	109	EDB 14
49	RNG 16 G	110	RNG 8G
50	TCLK 0	111	RD SEL 1
51	RNG 32U	112	SPARE
52	TCLK 1	113	RD SEL 2
53	TCLK GND	114	SPARE
54	TCLK 2	115	WRT SEL 1
55	TCLK GND	116	SPARE
56	TCLK 3	117	WRT SEL 2
57	D/A ACT NOW	118	SPARE
58	(KEY)	119	(KEY)
59	IP 2	120	LDXR7C/0
60	+5V	121	+5V
61	+5V	122	+5V

TABLE D-9 BSAG 2 SLOT 19

PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND
2	GND	63	GND
3	LD A/D BS ADR CTR	64	
4	D/A DEL FF	65	LD D/A BS ADR CTR
5	D/A WC = 0	66	DEC RNG WD CTR
6		67	D/A BC = 0 DEL
7	A/D WC = 0	68	RST
8		69	
9	IP 3	70	IP 1
10		71	IP 2
11	RNG WC = 0	72	
12		73	D/A BUFF CNT BUFF 0
13	D/A BC = 0	74	1
14		75	2
15	A/D BC = 0	76	3
16	LOD 0	77	4
17	LOD 1	78	5
18	LOD 2	79	6
19	LOD 3	80	D/A BUFF CNT BUFF 7
20		81	
21	EDB 1	82	LOD 4
22	EDB 3	83	LOD 5
23	EDB 5	84	LOD 6
24	EDB 7	85	LOD 7
25	EDB 9	86	
26	EDB 11	87	0
27	EDB 13	88	
28	EDB 15	89	
29		90	EDB 0
30	SPARE 1	91	EDB 2
31	SPARE 2	92	EDB 4
32	SPARE 3	93	EDB 6
33	SPARE 4	94	EDB 8
34	SPARE 5	95	EDB 10
35		96	EDB 12
36	INIT 1	97	EDB 14
37	LDXR78/3	98	LDXR79/3
38	D/A ACT NOW	99	LDXR78/2
39	LDXR79/2	100	LDXR7A/5
40	A/D ACT NOW	101	RNG ACT NOW

PIN	SIGNAL	PIN	SIGNAL
41	BS ADR REG 1	102	BS ADR REG 0
42	BS ADR REG 3	103	BS ADR REG 2
43	BS ADR REG 5	104	BS ADR REG 4
44	BS ADR REG 7	105	BS ADR REG 6
45	BS ADR REG 9	106	BS ADR REG 8
46	BS ADR REG 11	107	BS ADR REG 10
47	BS ADR REG 13	108	BS ADR REG 12
48	BS ADR REG 15	109	BS ADR REG 14
49		110	
50	ADR ADD 12	111	ADR ADD 13
51	ADR ADD 10	112	ADR ADD 11
52	ADR ADD 8	113	ADR ADD 9
53	ADR ADD 6	114	ADR ADD 7
54	ADR ADD 4	115	ADR ADD 5
55	ADR ADD 2	116	ADR ADD 3
56	ADR ADD 0	117	ADR ADD 1
57	ADR ADD 14	118	ADR ADD 15
58	(KEY)	119	(KEY)
59	LDXR79/1	120	LDXR78/1
60	+5V	121	+5V
61	+5V	122	+5V

TABLE D-10 BSAGC 1 SLOT 21

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41	BS ADR REG 5	102	BS ADR REG 4
2	GND	63	GND	42	BS ADR REG 7	103	BS ADR REG 6
3	EDB 1	64	A/D ACT NOW	43	BS ADR REG 9	104	BS ADR REG 8
4	EDB 3	65	RNG ACT NOW	44	BS ADR REG 11	105	BS ADR REG 10
5	EDB 5	66	D/A ACT NOW	45	BS ADR REG 13	106	BS ADR REG 12
6	EDB 7	67		46	BS ADR REG 15	107	BS ADR REG 14
					DEC RNG		
7	EDB 9	68		47	WD CTR	108	D/A BC = 0
					LD BS ADR		
8	EDB 11	69		48	REG	109	A/D BC = 0
9	EDB 13	70	LDXR78/0	49		110	
10	EDB 15	71	LDXR79/0	50	ADR ADD 12	111	ADR ADD 13
11		72	EDB 0	51	ADR ADD 10	112	ADR ADD 11
12		73	EDB 2	52	ADR ADD 8	113	ADR ADD 9
13		74	EDB 4	53	ADR ADD 6	114	ADR ADD 7
14		75	EDB 6	54	ADR ADD 4	115	ADR ADD 5
15		76	EDB 8	55	ADR ADD 2	116	ADR ADD 3
16		77	EDB 10	56	ADR ADD 0	117	ADR ADD 1
17		78	EDB 12	57	ADR ADD 14	118	ADR ADD 15
18		79	EDB 14	58	(KEY)	119	(KEY)
					MPX		MPX
19	LDSR7A/4	80	LDXR78/1	59	ENCODER HO	120	ENCODER LO
20	LDXR7A/3	81	LDXR79/1	60	+5V	121	+5V
21	SPARE 1	82		61	+5V	122	+5V
22	SPARE 2	83					
23	SPARE 3	84	BS ADR OUT				
24	SPARE 4	85	BSM ADR OUT				
25	SPARE 5	86					
26		87					
27	BS ADR 1	88	BS ADR 0				
28	BS ADR 3	89	BS ADR 2				
29	BS ADR 5	90	BS ADR 4				
30	BS ADR 7	91	BS ADR 6				
31	BS ADR 9	92	BS ADR 8				
32	BS ADR 11	93	BS ADR 10				
33	BSM ADR 1	94	BSM ADR 0				
34	BSM ADR 3	95	BSM ADR 2				
35	BSM ADR 5	96	BSM ADR 4				
36	GND	97					
			LD D/A BS				
37		98	ADR CTR				
			LD A/D BS				
38	BS ADR MPX 15	99	ADR CTR				
39	BS ADR REG 1	100	BS ADR REG 0				
40	BS ADR REG 3	101	BS ADR REG 2				

TABLE D-11 EDB/RTC SLOT 23

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	62	GND	41	CB 0	102	CB 1
2	GND	63	GND	42	CB 2	103	CB 3
3	EDB PO	64	EDB PAR ERR	43	CB 4	104	CB 5
4	SYS RST	65	EAB PAR	44	CB 6	105	CB 7
5	EDB 1	66	EDB 0	45	CB 8	106	CB 9
6	EDB 3	67	EDB 2	46	CB 10	107	CB 11
7	EDB 5	68	EDB 4	47	CB 12	108	CB 13
8	EDB 7	69	EDB 6	48	CB 14	109	CB 15
9	EDB 9	70	EDB 8	49		110	
10	EDB 11	71	EDB 10	50	CB 16	111	CB 17
11	EDB 13	72	EDB 12	51	CB 18	112	CB 19
12	EDB 15	73	EDB 14	52	CB 20	113	CB 21
13	EAB 4	74	EAB 0	53	CB 22	114	CB 23
14	EAB 6	75	EAB 2	54	CB 24	115	CB 25
15	EAB 6	76	EAB 1	55	CB 26	116	CB 27
16	EAB 5	77	EAB 3	56	CB 28	117	CB 29
17	RNG HO OUT	78	EDB ACK	57	CB 30	118	CB 31
18	RNG MO OUT	79	EDB P1	58	(KEY)	119	(KEY)
19	LDXR79/2	80	EDB SEL	59		120	
20	RNG LO OUT	81	EDB R/W	60	+5V	121	+5V
21	LDXR79/3	82	LDXR78/1	61	+5V	122	+5V
22	LDXR7A/0	83	LDXR78/2				
23	LDXR7A/3	84	RDXR78/0				
24	LDXR7A/1	85	LDXR78/3				
25	LDXR7A/4	86	LDXR78/0				
26	LDXR7A/2	87	LDXR79/0				
27	LDXR7A/5	88	LDXR7C/0				
28	LDXR7C/1	89	LDXR79/1				
29	OSC RST IN	90	STATUS OUT				
30	MANUAL RST	91	RTC ACT				
31	ARTC	92	RTC				
32	PINGTA+	93	PINGTB+				
33	PINGTA–	94	PINGTB–				
34	12.6 MHz	95	PINGTC+				
35	12.6 MHz GND	96	PINGTC–				
36	SPARE 4	97	PINGTD+				
37	SPARE 5	98	PINGTD–				
			EDB ACK				
38	SPARE 1	99	PRE BUS				
39	SPARE 2	100	RSTXR7B/0				
40	SPARE 3	101	LDXR7A/1				

APPENDIX E

FINAL OSCILLOSCOPE TRACES OF THE OSCBH D/A OUTPUTS AFTER SUCCESSFUL COMPLETION OF BASIC DIAGNOSTICS

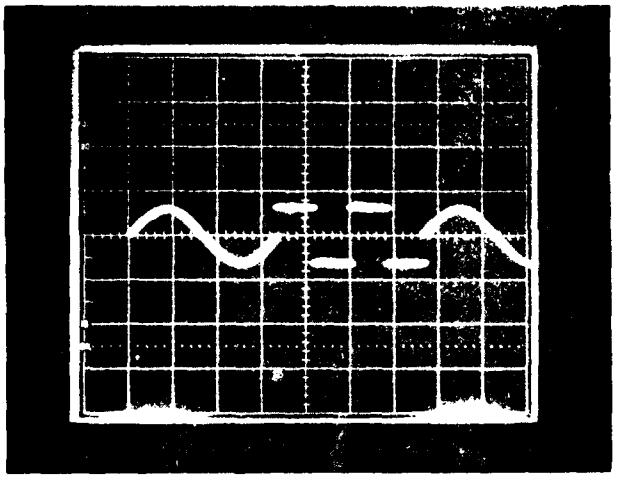

FIGURE E 1

D A CHANNELS
2, 4, 7, 10, 13, 16, 19, 22

HORZ 50MS CM
VERT IV CM

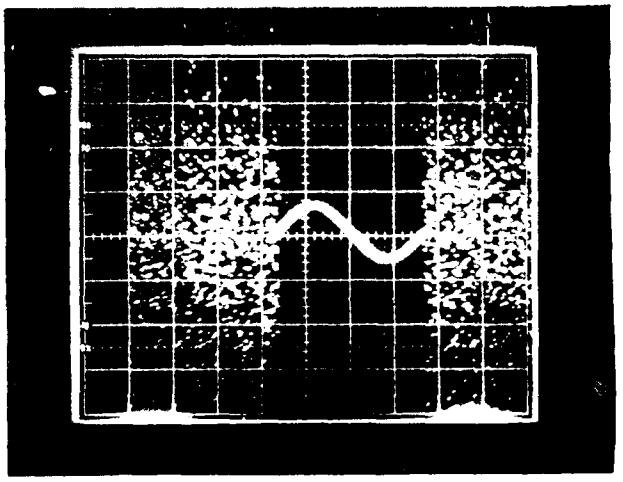

FIGURE E 2

D A CHANNELS
2, 5, 8, 11, 14, 17, 20, 23

HORZ 50MS CM
VERT IV CM

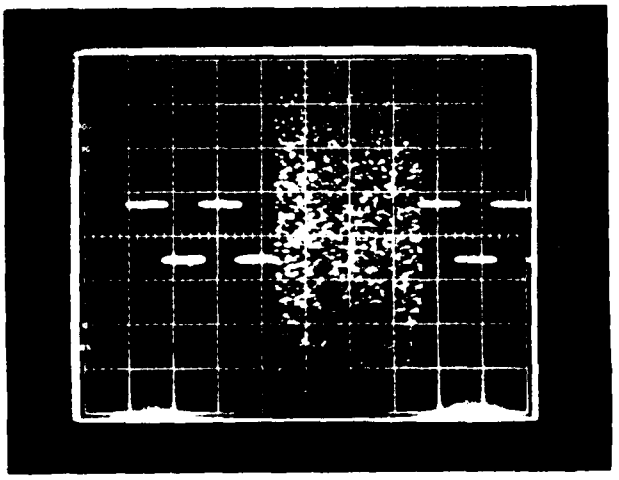

FIGURE E 3

D A CHANNELS
3, 6, 9, 12, 15, 18, 21, 24

HORZ 50MS CM
VERT IV CM

APPENDIX F

SOURCE LISTING OF OSCBH DIAGNOSTIC PROGRAM

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

                                     1          PRINT  OFF
                                   444 *
000000                             445 OSCTST2  CSECT
                                   446 *
000000                             447 APTASK8  EQU    *
                                   448          ENTRY  APTASK8
000000 E9FD                        449          BALR   R7,0
000001                             450          USING  *,R7
                                   451 *
000001 1CFF                        452          XRA    A7L,A7L
000002 5910006A                    453          LIM    A1,X'006A'          ADDR OF OLD OSC PSW
000004 6D1F2258                    454          MM     A1,2,OLDPSW         STORE OSC PSW
000006 451F0269                    455          L      A1,NEWPSWA          MOVE IN NEW PSW
00000A 6D10206A                    456          MM     A1,2,X'006A'
                                   457 *
                                   458 * INITIAL STATUS READ
                                   459 *
00000A F5008000                    460          SSM    X'8000'             MACHINE CHECK IN + ENABLED
00000C 1C11                        461          XRA    A0L,A0L
00000D 1900007C                    462          LIMA   A0H,X'007C'
00000F 32010004                    463          DIAG   A0H,A0L,4
000011 19000078                    464 L1       LIMA   A0H,X'0078'         STATUS READ
000013 32010003                    465          DIAG   A0H,A0L,3           DUMMY READ
000015 32010003                    466          DIAG   A0H,A0L,3           READ STATUS
000017 0AF00001                    467          CIMA   A7L,1
                                   468          BE     L1
000019 E48F0010                    469+ BC CC8,L1 BRANCH IF FIRST OPERAND = SECOND OPERAND
00001B 1E10200C                    470          XIMA   A0L,X'200C'         COMPLEMENT ONES
                                   471          BEZ    L2
00001D E48F0024                    472+ BC CC8,L2 BRANCH IF OPERAND OR RESULT = ZERO
00001F 32000000                    473          DIAG   0,0,0               STOP
000021 EA0F0024                    474          B      ,L2
000023 32000000                    475 OSCED8   DIAG   0,0,0
                                   476 *
                                   477 * READ WHATEVER SEEDED INTO RNG
                                   478 *
000025 1900007A                    479 L2       LIMA   A0H,X'007A'         RNG 1ST WORD
000027 32010003                    480          DIAG   A0H,A0L,3
000029 1900007A                    481          LIMA   A0H,X'007A'         RNG 2ND WORD
00002B 32010003                    482          DIAG   A0H,A0L,3
00002D 1900007A                    483          LIMA   A0H,X'007A'         RNG 3RD WORD
00002F 32010003                    484          DIAG   A0H,A0L,3
000031 0AF00002                    485          CIMA   A7L,2
                                   486          BE     L2
000033 E48F0024                    487+ BC CC8,L2 BRANCH IF FIRST OPERAND = SECOND OPERAND
                                   488 *
                                   489 * PUT IN NEW PSW
                                   490 *
000035 5910007C                    491          LIM    A1,X'007C'
000037 6D1F2263                    492          MM     A1,2,OLDISC
```

@916H

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(1 OF 11)

```
   LOC OBJECT CODE        STMT SOURCE STATEMENT

000039 451F0271            491          L      A1,NEWPSWB          ADDRESS OF OSC INT PSW
00003B 6D10207C            494          MM     A1,2,X'007C'
                           495 *
                           496 * START RNG
                           497 *
00003D 1900007B            498 L3       LIMA   A0H,X'007B'
00003F 32010003            499          DIAG   A0H,A0L,3
000041 5D1F2281            500          LM     A1,2,RNGPM1         LOAD FIRST RNG STATE
000043 1900007A            501          LIMA   A0H,X'007A'         RNG ADDRESS
000045 32020004            502          DIAG   A0H,A1H,4           H.O. RNG STATE
000047 32030004            503          DIAG   A0H,A1L,4           M.O. RNG STATE
000049 32040004            504          DIAG   A0H,A2H,4           L.O. RNG STATE
00004B 32050004            505          DIAG   A0H,A2L,4           H.O. ADDRESS
00004D 32060004            506          DIAG   A0H,A3H,4           L.O. ADDRESS
00004F 32070004            507          DIAG   A0H,A3L,4           LENGTH
                           508 *
                           509 * READ OUT RNG STATE
                           510 *
000051 1900007B            511 RNG1     LIMA   A0H,X'007B'
000053 32010003            512          DIAG   A0H,A0L,3
000055 1900007A            513          LIMA   A0H,X'007A'
000057 32080003            514          DIAG   A0H,A4H,3           READ WORD 0
000059 32090003            515          DIAG   A0H,A4L,3           READ WORD 1
00005B 320A0003            516          DIAG   A0H,A5H,3           READ WORD 2
00005D 0AF00003            517          CIMA   A7L,3
                           518          BE     L3
00005F E48F003C            519* BC CC8,L3 BRANCH IF FIRST OPERAND = SECOND OPERAND
000061 0882                520          CRA    A4H,A1H             H.O. TEST
                           521          BE     RNG2
000062 E48F0065            522* BC CC8,RNG2 BRANCH IF FIRST OPERAND = SECOND OPERAND
000064 32000000            523          DIAG   0,0,0               STOP
000066 0893                524 RNG2     CRA    A4L,A1L             M.O. TEST
                           525          BE     RNG3
000067 E48F006A            526* BC CC8,RNG3 BRANCH IF FIRST OPERAND = SECOND OPERAND
000069 32000000            527          DIAG   0,0,0               STOP
00006B 08A4                528 RNG3     CRA    A5H,A2H             L.O. TEST
                           529          BE     STRNGA
00006C E48F006F            530* BC CC8,STRNGA BRANCH IF FIRST OPERAND = SECOND OPERAND
00006E 32000000            531          DIAG   0,0,0               STOP
                           532 *
000070 1900007B            533 STRNGA   LIMA   A0H,X'007B'
000072 32010003            534          DIAG   A0H,A0L,3
                           535 *
                           536 *OSC ADDRESS RESET TEST
                           537 *
000074 5D1F1281            538          LM     A1,1,RNGPM1
000076 1900007A            539          LIMA   A0H,X'007A'
000078 19000063            540          LIMA   A3H,X'0063'         AEC STATUS
00007A 32020004            541          DIAG   A0H,A1H,4           RNG HD STATE
00007C 32670003            542          DIAG   A3H,A3L,3           READ AEC STATUS
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(2 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

0000?E 32030004                    543          DIAG   A0H,A1L,4              RNG MO STATE
000080 32040004                    544          DIAG   A0H,A2H,4              RNG LO STATE
000082 1900007B                    545          LIMA   A0H,X'007B'            DUMMY
000084 32010003                    546          DIAG   A0H,A0L,3              READ
000086 1900007A                    547          LIMA   A0H,X'007A'            RNG ADDRESS
000088 32080003                    548          DIAG   A0H,A4H,3              READ HO STATE
00008A 32090003                    549          DIAG   A0H,A4L,3              READ MO STATE
00008C 320A0003                    550          DIAG   A0H,A5H,3              READ LO STATE
00008E 0A93                        551          CRA    A4L,A1L                MO TEST
                                   552          BE     LOTST
00008F E48F0092                    553+ BC CC8,LOTST BRANCH IF FIRST OPERAND = SECOND OPERAND
000091 32000000                    554          DIAG   0,0,0                  FAULT
000093 0A44                        555 LOTST    CRA    A5H,A2H                IO TEST
                                   556          BE     BLKTST
000094 E48F0097                    557+ BC CC8,BLKTST BRANCH IF FIRST OPERAND = SECOND OPERAND
000096 32000000                    558          DIAG   0,0,0                  FAULT
                                   559 *
                                   560 * TEST OVER
                                   561 *
000098 1900007B                    562 BLKTST   LIMA   A0H,X'007B'
00009A 32010003                    563          DIAG   A0H,A0L,3
                                   564          MLDSTC
00009C 0900                        565+ TTSR 0
00009D E42F009B                    566+  BC CC2,*-1
00009F 19R00001                    567          LIMA   A5L,1
0000A1 5D1F22R1                    568          LM     A1,2,RNGPM1
0000A3 1C99                        569          XRA    A4L,A4L
0000A4 219F0290                    570          STA    A4L,MSK
0000A6 45DF0257                    571          L      R5,RNGTESA
0000A8 E9ED                        572          BALR   R6,R5
                                   573 *
                                   574 * GENERATE SQUARE WAVE
                                   575 *
0000A9 454F0295                    576          L      A4,SQWPTR
0000AB 05DF0299                    577          LA     A6L,C256
0000AD 1CFF                        578          XRA    A7L,A7L
0000AE 05AF0298                    579          LA     A5H,C1000
0000B0 11RA                        580          LCRA   A5L,A5H
0000B1 21A47000                    581 LP1      STA    A5H,0,A4,X7
0000B3 21A47200                    582          STA    A5H,512,A4,X7
0000B5 21A47100                    583          STA    A5L,256,A4,X7
0000B7 21A47300                    584          STA    A5L,768,A4,X7
0000B9 02F00001                    585          AIMA   A7L,1
0000BB E5DF00B0                    586          BCT    A6L,LP1
                                   587 *
                                   588 * GENERATE SINEWAVE
                                   589 *
0000BD 455F0297                    590          L      A5,SINPTR
0000BF 05CF029A                    591          LA     A6H,C1024
0000C1 1CDD                        592          XRA    A6L,A6L
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(3 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

0000C2 454F02C1                    593          L      A4,DELTAS
0000C4 4400                        594          SR     A0,A0
0000C5 452F029C                    595          L      A2,C2000
0000C7 21056000                    596 LP2      STA    A0H,0,A5,X6
0000C9 4110                        597          LR     A1,A0
0000CA 4132                        598          LR     A3,A2
0000CH 0C0A                        599          MRA    A0H,A4H
0000CC 0C29                        600          MRA    A1H,A4L
0000CD 0C4A                        601          MRA    A2H,A4H
0000CE 0C69                        602          MRA    A3H,A4L
0000CF 4003                        603          AR     A0,A3
0000D0 4000                        604          AR     A0,A0
0000D1 4421                        605          SR     A2,A1
0000D2 4022                        606          AR     A2,A2
0000D3 02D00001                    607          AIMA   A6L,1
0000D5 E5CF00C6                    608          BCT    A6H,LP2
                                   609 *
                                   610 * LOAD SQUARE AND SINE WAVEFORMS INTO MEMORY
                                   611 *
0000D7 19F00009                    612          LIMA   A7L,9
0000D9 D50F029F                    613 DTC8L    XDT    ,DTATC8
                                   614          MLDSTC
0000D8 D900                        615+ TTSR 0
0000DC E42F00DA                    616+  BC CC2,*-1
0000DE 05DF02A1                    617          LA     A6L,DTATCR+2
0000E0 02D01800                    618          AIMA   A6L,X'1800'
0000E2 21DF02A1                    619          STA    A6L,DTATCR+2
0000E4 E5FF00D8                    620          BCT    A7L,DTC8L
                                   621 *
                                   622 * FILL IN RNG BLOCKS
                                   623 *
0000E6 19F00008                    624          LIMA   A7L,8                  ENTER BLOCKS TO BE FILLED
0000EA 5D1F22B5                    625 DRNGL    LM     A1,2,RNGDA             LOAD RNG PARAMETERS
0000EA 1CBB                        626          XRA    A5L,A5L                CLEAR FOR RNGTES (RUN)
0000EB 1C99                        627          XRA    A4L,A4L
0000EC 219F029D                    628          STA    A4L,MSK
0000EE 45DF0257                    629          L      B5,RNGTESA
0000F0 E9ED                        630          BALR   B6,B5
0000F1 055F0289                    631          LA     A2L,RNGAD              GET RNG ADDRESS
0000F3 02500300                    632          AIMA   A2L,X'0300'            ADD 300 DW TO ADDRESS
0000F5 215F0289                    633          STA    A2L,RNGAD              RESTORE PARAMETER
0000F7 E5FF00E7                    634          BCT    A7L,DRNGL              CHECK IF DONE
                                   635 *
                                   636 * TEST RNG WITH D/A'S RUNNING BUT NOT INTERRUPTING PROGRAM
                                   637 *
0000F9 F5008000                    638          SSM    X'8000'                ALLOW NO INTERRUPTS
                                   639 *                                      TO BE RECOGNIZED
0000FB 5D1F12B1                    640          LM     A1,1,DAPMA             LOAD D/A PARAMETERS
0000FD 19000078                    641          LIMA   A0H,X'0078'            D/A ADDRESS
0000FF 32020004                    642          DIAG   A0H,A1H,4              M.O. ADDRESS
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(4 OF 11)

```
   LOC OBJECT CODE        STMT SOURCE STATEMENT

000101 32030004          643          DIAG   A0H,A1L,4          L.O. ADDRESS
000103 32040004          644          DIAG   A0H,A2H,4          COUNT
000105 32050004          645          DIAG   A0H,A2L,4          LENGTH
000107 19208000          646          LIMA   A1H,X'8000'       INIT D/A MODE
000109 19304100          647          LIMA   A1L,X'4100'       INIT CLOCK
00010B 1900007C          648          LIMA   A0H,X'007C'       MODE/CLOCK ADDRESS
00010D 32020004          649          DIAG   A0H,A1H,4
00010F 32030004          650          DIAG   A0H,A1L,4          WRITE CLOCK
                         651 *
                         652 * TURN ON RNG WITH TEST
                         653 *
000111 19A00001          654          LIMA   A5L,1              BLOCK TEST MODE
000113 5D1F2281          655          LM     A1,2,RNGPM1        LOAD IN PARS FOR 1ST BLOCK
000115 19908000          656          LIMA   A4L,X'8000'
000117 219F029D          657          STA    A4L,MSK
000119 45DF0257          658          L      B5,RNGTESA
00011B E9ED              659          BALR   B6,B5
                         660 *
                         661 * TESTS OK
                         662 *
00011C 19900005          663          LIMA   A4L,5              DATA TRANSFER WHILE D/A S ON
00011E 058F02A5          664 LSTC     XDT    ,DATCB1            DATA TRANSFER FROM PS TO BS
                         665          WLDSTC
000120 D900              666+ TTSR 0
000121 E42F011F          667+  BC CC2,*-1
000123 058F02AB          668          XDT    *,DATCB2           DATA TRANSFER FROM BS TO PS
                         669          WLDSTC
000125 D900              670+ TTSR 0
000126 E42F0124          671+  BC CC2,*-1
000128 19500400          672          LIMA   A2L,1024
00012A 9C77              673          XRR    B3L,B3L
00012B 459F0295          674          L      B1,SQWPTR
00012D 45AF0AC3          675          L      B2,TEMP1
00012F 45693000          676 LTEST    L    A6,0,B1,X'3'
000131 455A3000          677          L      A5,0,B2,X'3'
000133 4856              678          CR     A5,A6
                         679          BE     LBS
000134 E48F0137          680+ BC CC8,LBS BRANCH IF FIRST OPERAND = SECOND OPERAND
000136 32000000          681          DIAG   0,0,0
000138 82700002          682 LBS      AIMB   B3L,2
00013A E55F012E          683          BCT    A2L,LTEST
00013C E59F0110          684          BCT    A4L,LSTC
00013E 5D1F12AA          685          LM     A1,1,DAPMB
000140 19000078          686          LIMA   A0H,X'0078'
000142 32020004          687          DIAG   A0H,A1H,4
000144 32030004          688          DIAG   A0H,A1L,4
000146 32040004          689          DIAG   A0H,A2H,4
000148 32050004          690          DIAG   A0H,A2L,4
                         691 *
                         692 * RESET INTERRUPTS
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(5 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

                                  693 *
000148 19A80092                   694          LIMA    A5H,X'0082'          CONTROL CHANNEL ADDRESS
00014C DAA0                       695          TCH     A5H                  CLEAR INTERRUPTS
                                  696 *
                                  697 * WAIT FOR OSC INTERRUPT
                                  698 *
00014D 19B8070A                   699          LIMA    A5L,X'070A'
00014F 5C11                       700          XR      A1,A1
000150 F5000020                   701 ENOSC    SSM     X'0020'              OSC INTERRUPT ENABLED
000152 5C33                       702 WAITINT  XR      A3,A3
000153 454F020F                   703          L       A4,DELAY
000155 632F0156                   704          LSL     A2,LL1
000157 42300001                   705 LL1      AIM     A3,1
000159 E192                       706          BCTR    A4L,A2
00015A 4133                       707          LR      A3,A3
00015B 4133                       708          LR      A3,A3
00015C 4133                       709          LR      A3,A3
00015D E182                       710          BCTR    A4H,A2
00015E F5000000                   711          SSM     0
000160 32000000                   712          DIAG    0,0,0
                                  713 *
                                  714 * INTERRUPT ROUTINE
                                  715 *
000162 19000078                   716 OSCINT   LIMA    A0H,X'0078'          DUMMY READ
000164 32010003                   717          DIAG    A0H,A0L,3
000166 0A300000                   718          CIMA    A1L,0
                                  719          BE      ADDINC
00016A E48F016F                   720+ BC CC8,ADDINC BRANCH IF FIRST OPERAND = SECOND OPERAND
00016A 19208000                   721          LIMA    A1H,X'8000'
00016C 06300001                   722          SIMA    A1L,1
00016E EA0F0173                   723          B       ,SWAP
000170 19208100                   724 ADDINC   LIMA    A1H,X'8100'
000172 02300001                   725          AIMA    A1L,1
000174 1C77                       726 SWAP     XRA     A3L,A3L
000175 19000078                   727          LIMA    A0H,X'0078'
000177 32070004                   728          DIAG    A0H,A3L,4
000179 32020004                   729          DIAG    A0H,A1H,4
00017B E58F0151                   730          BCT     A5L,WAITINT
00017D                            731 L5       EQU     *
00017D F5000000                   732          SSM     0
00017F 5900007C                   733          LIM     A0,X'007C'
000181 32100004                   734          DIAG    A0L,A0H,4
000183 32100004                   735          DIAG    A0L,A0H,4
000185 DAA0                       736          TCR     A5H
000186 451F0259                   737          L       A1,OLDPSWA
00018A 6D10206A                   738          MM      A1,2,X'006A'
00018A 451F0261                   739          L       A1,OLDISCA
00018C 6D10207C                   740          MM      A1,2,X'007C'
00018E F5008000                   741          SSM     X'8000'
                                  742          XWAIT   ECBTASK8
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(6 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

                                   744+***** MACRO XWAIT ***** 06/02/76 *****

                                   747+**
                                   748+** DATE OF LAST CHANGE ***** 01/06/77 *****
                                   749+** DATE OF LAST CHANGE ***** 02/11/77 *****
                                   750+** DATE OF LAST CHANGE ***** 10/28/77 *****
                                   751+** DATE OF LAST CHANGE ***** 11/11/77 *****
000190 5910000E                    752+ LIM A1,14 LOAD DISPLACEMENT VALUE
000192 1A20B000                    753+  OIMA A1H,X'B000' SET IN OPTION BIT
000194 FC00                        754+  XCR 0 ISSUE WAIT XCR

                                   756+***** END MACRO XWAIT *****

                                   758 *
                                   759 *
                                   760 RNGTES   SBNTR
000195 E000                        761+  CNOP
000196 69ED1004                    762+RNGTES STM B6,1,4,B5
00019A EA0D000B                    763+  B ,8,B5
00019A                             764+  DS 2F
00019E 41FD                        765+  LR B7,B5
00019A                             766+  USING *-9,B7
                                   767 *
                                   768 * A5L =1 IF BLOCK TEST
                                   769 * A5L = 0 IF RUN ONLY
                                   770 *
00019F 1900007A                    771          LIMA   A0H,X'007A'
0001A1 32020004                    772          DIAG   A0H,A1H,4
0001A3 32030004                    773          DIAG   A0H,A1L,4
0001A5 32040004                    774          DIAG   A0H,A2H,4
0001A7 32050004                    775          DIAG   A0H,A2L,4
0001A9 32060004                    776          DIAG   A0H,A3H,4
0001AB 32070004                    777          DIAG   A0H,A3L,4
0001AD 0AB00001                    778          CIMA   A5L,1
                                   779          BE     STRNG
0001AF E4BF001D                    780+ BC CC8,STRNG BRANCH IF FIRST OPERAND = SECOND OPERAND
0001B1 EA0F0020                    781          B      ,STRUNO
0001B3 1C99                        782 STRNG    XRA    A4L,A4L                 BLOCK COUNT
0001B4 1CCC                        783          XRA    A6H,A6H                 MODE ID, AGH=0,1,2=8G,16G,32U
0001B5 1CDD                        784          XRA    A6L,A6L                 BLOCK ID
0001B6 19101A00                    785 STRUNO   LIMA   A0L,X'1A00'             RNG AG MODE
0001B8 05AF0108                    786 REGRNG   LA     A4H,MSK
0001BA 1A18                        787          ORA    A0L,A4H
0001BA 1900007C                    788          LIMA   A0H,X'007C'
0001BD 32010004                    789          DIAG   A0H,A0L,4               START RNG
                                   790 *
                                   791 * CHECK FOR BUSY
                                   792 *
0001BF 1900007B                    793          LIMA   A0H,X'007B'             LOAD STATUS ADDRESS
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(7 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

0001C1 32010003                    794          DIAG   A0H,A0L,3              READ STATUS
0001C3 38102000                    795          TIMA   A0L,X'2000'
                                   796          BANZ   WAIT                   SHOULD = 0
0001C5 E4AF0033                    797+ BC CC8,WAIT BRANCH IF LOGICAL RESULT HAS NO BITS SET
0001C7 12000000                    798          DIAG   0,0,0                  STOP
                                   799 *
                                   800 * WAIT FOR DONE
                                   801 *
0001C9 19E003E8                    802 WAIT     LIMA   A7H,1000               SET FOR TIMEOUT
0001CB 32010003                    803 WAIT2    DIAG   A0H,A0L,3              CONTINUE READING STATUS
0001CD 38102000                    804          TIMA   A0L,X'2000'            CHECK RNG DONE
                                   805          BANP   CONT                   EXIT IF DONE
0001CF ECAF003D                    806+ BNC CC8,CONT BRANCH IF LOGICAL RESULT HAS ANY BIT SET
0001D1 E5EF0035                    807          BCT    A7H,WAIT2              DECR LOOP CTR NOT DONE
0001D3 1E102000                    808 CONT     XIMA   A0L,X'2000'            RNG DONE SET BIT 2
0001D5 38103C00                    809          TIMA   A0L,X'3C00'
                                   810          BANZ   L23
0001D7 E4AF0045                    811+ BC CC8,L23 BRANCH IF LOGICAL RESULT HAS NO BITS SET
0001D9 32000000                    812          DIAG   0,0,0
0001DB 0AA00000                    813 L23      CIMA   A5L,0
                                   814          BE     RNEND
0001DD E4AF008E                    815+ BC CC8,RNEND BRANCH IF FIRST OPERAND = SECOND OPERAND
0001DF 1900007A                    816          LIMA   A0H,X'007A'            RNG FIRST WORD
0001E1 32020003                    817          DIAG   A0H,A1H,3              READ MD SEED
0001E3 32030003                    818          DIAG   A0H,A1L,3              READ MD SEED
0001E5 32040003                    819          DIAG   A0H,A2H,3              READ LO SEED
0001E7 1900007B                    820          LIMA   A0H,X'007B'
0001E9 32010003                    821          DIAG   A0H,A0L,3
0001EB 0AD00000                    822          CIMA   A6L,0                  CHECK IF 1ST OR 2ND BLOCK
                                   823          BE     SECN                   IF FIRST, JUMP
0001ED E4AF005D                    824+ BC CC8,SECN BRANCH IF FIRST OPERAND = SECOND OPERAND
0001EF 691F10EB                    825          STM    A1,1,PARAMB            STORE SECOND BLOCK SEED
0001F1 EA0F005F                    826          B      ,INK                   BRANCH TO CONTINUE
0001F3 691F10E4                    827 SECN     STM    A1,1,PARAMA            STORE SEED OF FIRST BLOCK
0001F5 02D00001                    828 INK      AIMA   A6L,1                  ADD 1 TO BLOCK CTR
0001F7 0AD00001                    829          CIMA   A6L,1                  FIRST BLOCK
                                   830          BNE    L24                    BOTH BLOCKS DONE,JUMP
0001F9 ECAF00A9                    831+ BNC CC8,L24 BRANCH IF FIRST OPERAND NOT = SECOND
                                   832 *
                                   833 * GENERATE SECOND BLOCK
                                   834 *
0001FB 5D1F20F2                    835          LM     A1,2,RNGPM2            LOAD PARS FOR 2ND BLOCK
0001FD 0AC00000                    836 RELD     CIMA   A6H,0                  8G MODE
                                   837          BE     RNG8G                  JUMP TO 8G
0001FF E4AF0077                    838+ BC CC8,RNG8G BRANCH IF FIRST OPERAND = SECOND OPERAND
000201 0AC00001                    839          CIMA   A6H,1                  16G MODE
                                   840          BE     RNG16G                 JUMP
000203 E4AF0073                    841+ BC CC8,RNG16G BRANCH IF FIRST OPERAND = SECOND OPERAND
000205 19101200                    842          LIMA   A0L,X'1200'            32 UNIFORM
000207 EA0F0079                    843          B      ,RNGPAR                JUMP
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(8 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

000209 19101400                    844 RNG16G   LIMA    A0L,X'1400'          16 MODE
00020B EA0F0079                    845          B       ,RNGPAR              JUMP
00020D 19101A00                    846 RNG8G    LIMA    A0L,X'1A00'          8 MODE
                                   847 *
                                   848 * LOAD PARAMETERS
                                   849 *
00020F 1900007A                    850 RNGPAR   LIMA    A0H,X'007A'          ADDRESS OF RNG
000211 32020004                    851          DIAG    A0H,A1H,4            H.O. RNG STATE
000213 32030004                    852          DIAG    A0H,A1L,4            H.O. RNG STATE
000215 32040004                    853          DIAG    A0H,A2H,4            L.O. RNG STATE
000217 32050004                    854          DIAG    A0H,A2L,4            H.O. RNG ADDRESS
000219 32060004                    855          DIAG    A0H,A3H,4            L.O. ADDRESS
00021B 32070004                    856          DIAG    A0H,A3L,4            LENGTH
00021D EA0F0022                    857          B       ,BEGRNG              JUMP TO RNG BEGIN
                                   858 *
                                   859 * BLOCK TESTING
                                   860 *
00021F D50F00F8                    861 L24      XDT     ,TCB1                START TRANSFER OF RNG
                                   862          MLDSTC
000221 D900                        863+ TTSR 0
000222 E42F008B                    864+  BC CC2,*-1
000224 9C77                        865          XRR     B3L,B3L              CLEAR LOOP INDEX
000225 19900200                    866          LIMA    A4L,512
000227 45AF092E                    867          L       B2,TEMP1
000229 451A3000                    868 L26      L       A1,0,B2,X3
00022B 452A3400                    869          L       A2,1024,B2,X3
00022D 4A12                        870          CR      A1,A2
                                   871          BE      L30                  BRANCH IF EQUAL
00022F E48F009C                    872+ BC CC8,L30 BRANCH IF FIRST OPERAND = SECOND OPERAND
                                   873 *
                                   874 * FAULT
                                   875 *
000231 32000000                    876          DIAG    0,0,0                STOP AND CHECK BITS
000233 8A700002                    877 L30      AIMB    B3L,2                BUMP INDEX
000235 E59F0093                    878          BCT     A4L,L26              BRANCH ON COUNT
000237 5D1F10E4                    879          LM      A1,1,PARAMA          LOAD FIRST STATE
00023B 5D3F10E8                    880          LM      A3,1,PARAMB          LOAD SECOND STATE
00023A 0A26                        881          CRA     A1H,A3H              COMPARE H.O.
                                   882          BE      TST2                 IF EQUAL, BRANCH
00023B E48F00A9                    883+ BC CC8,TST2 BRANCH IF FIRST OPERAND = SECOND OPERAND
00023D 32000000                    884          DIAG    0,0,0
00023F 0A37                        885 TST2     CRA     A1L,A3L              COMPARE H.O.
                                   886          BE      TST3                 IF EQUAL, BRANCH
000240 E48F00AE                    887+ BC CC8,TST3 BRANCH IF FIRST OPERAND = SECOND OPERAND
000242 32000000                    888          DIAG    0,0,0
000244 0A48                        889 TST3     CRA     A2H,A4H              COMPARE L.O.
                                   890          BE      TSTM                 IF EQUAL, BRANCH
000245 E48F0083                    891+ BC CC8,TSTM BRANCH IF FIRST OPERAND = SECOND OPERAND
000247 32000000                    892          DIAG    0,0,0
000249 02C00001                    893 TSTM     AIMA    A6H,1                INCREMENT MODE
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(9 OF 11)

```
   LOC OBJECT CODE                STMT SOURCE STATEMENT

000248 0AC00003                    894          CIMA   A6H,3
                                   895          BE     RNEND                    YES, BRANCH
000240 E6AF00AE                    896+ BC CC8,RNEND BHANCH IF FIRST OPERAND = SECOND OPERAND
00024F 5D1F20EC                    897          LM     A1.2,RNGPM1              NO, RELOAD
000251 1C0D                        898          XRA    A6L,A6L
000252 E40F0067                    899          B      ,RELO
                                   900 *
                                   901 RNEND    SBRTN
000254 41DF                        902+RNEND LR B5,B7
000255 5DED1004                    903+  LM B6,1,4,B5
000257 EE0E                        904+  BR ,B6
                                   905 *
000258                             906          DS     0F
000258 00000196                    907 RNGTESA  DC     A(RNGTES)
00025A 0000025C                    908 OLDPSWA  DC     A(OLDPSW)
00025C                             909 OLDPSW   DS     3F
000262 00000264                    910 OLDISCA  DC     A(OLDISC)
000264                             911 OLDISC   DS     3F
000264 0000026C                    912 NEWPSWA  DC     A(NEWPSW)
00026C 80000000                    913 NEWPSW   DC     X'80000000'
00026E 0000A000                    914          DC     X'0000A000'
000270 DD000023                    915          DC     P'X'DD',A,0,4,OSCEDB,20'
000272 00000274                    916 NEWPSWB  DC     A(NPSWOS)
000274 80000000                    917 NPSWOS   DC     X'80000000'
000276 00000020                    918          DC     X'00000020'
000278 DD000142                    919          DC     P'X'DD',A,0,4,OSCINT,20'
00027A                             920 PARAMA   DS     2F
00027E                             921 PARAMB   DS     2F
000282 45C789AE                    922 RNGPM1   DC     X'45C789AE'
000284 E4000000                    923          DC     X'E4000000'
000286 A0000100                    924          DC     X'A0000100'
00028A 45C789AE                    925 RNGPM2   DC     X'45C789AE'
00028A E4000000                    926          DC     X'E4000000'
00028C A1000100                    927          DC     X'A1000100'
00028E                             928          DS     0F
00028E F01A                        929 TCB1     DC     X'F01A'
00028F 7FE50000                    930          DC     P'1023,11,327680,21'
000291 00108000                    931          DC     P'1,12,X'8000',20'
000294                             932 TSTID    DS     1F
000296 000002C4                    933 SQWPTR   DC     A(SQWVA)
000298 000006C4                    934 SINPTR   DC     A(SINWV)
00029A 0100                        935 C256     DC     H'256'
00029B 0400                        936 C1024    DC     H'1024'
00029C 1000                        937 C1000    DC     X'1000'
00029D 2000                        938 C2000    DC     X'2000'
00029E                             939 MSK      DS     1H
0002A0                             940          DS     0F
0002A0 F00A                        941 DTATCB   DC     X'F008'
0002A1 3FE40000                    942          DC     P'511,11,262144,21'
0002A3 00100204                    943          DC     P'1,12,PSBUFF,20'
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(10 OF 11)

```
   LOC OBJECT CODE                  STMT SOURCE STATEMENT

0002A6                               944          DS     0F
0002A6 F00A                          945 DATCB1   DC     X'F008'
0002A7 3FF60000                      946          DC     P'51',11,393216,2I'
0002A9 001002C4                      947          DC     P'1',12,PSBUFF,20'
0002AC                               948          DS     0F
0002AC F01A                          949 DATCB2   DC     X'F01A'
0002AD 7FEA0000                      950          DC     P'1023',11,393216,2I'
0002AF 00100000                      951          DC     P'1',12,X'A000',20'
0002B2                               952          DS     0F
0002B2 00008000                      953 DAPMA    DC     X'0000A000'
0002B4 00030100                      954          DC     X'00030100'
0002B6 45C789AE                      955 RNGDA    DC     X'45C789AE'
0002B8 E4000000                      956          DC     X'E4000000'
0002BA A2000100                      957 RNGAD    DC     X'A2000100'
0002BC 0000A000                      958 DAPMB    DC     X'0000A000'
0002BE 00180100                      959          DC     X'00180100'
0002C0 00050000                      960 DELAY    DC     X'00050000'
0002C2 7FFF00C9                      961 DELTAS   DC     X'7FFF00C9'
0002C4                               962          DS     0F
0002C4                               963 PSBUFF   EQU    *
0002C4                               964 SQWVA    DS     512F
0006C4                               965 SINWV    DS     512F
008000                               966 TEMP1A   EQU    X'8000'
000AC4 00008000                      967 TEMP1    DC     P'TEMP1A',32'
                                     968 *
                                     969          END
```

FIGURE F-1 DIAGNOSTIC SOURCE LISTING
(11 OF 11)

APPENDIX G

SIN X/X FILTER CHARACTERISTICS

The Digital-to-Analog Converter (DAC) required a low-pass filter to correct the sin x/x attenuation inherent in the converter. The low-pass filter specifications are given in Table G-1. Figure G-1 is the schematic of the filter used to provide this correction function to the DAC waveform. The response of the filter can be found in Figure G-2. The low pass filter boards containing eight filters per board were inserted into the Output Signal Conditioner/Applications Hardware (OSCAH) appendix.

TABLE G-1 SIN X/X FILTER CHARACTERISTICS

SPECIFICATIONS

FILTER TYPE:	4 POLE LOW-PASS FILTER
FILTER CHARACTERISTICS:	CORRECTS FOR $\frac{\text{SIN X}}{\text{X}}$ ATTENUATION OF D/A CONVERTER FROM DC TO 2.5 kHz WHERE 2.5 kHz is +2.6 dB (SEE PLOT)
CORRECTION ACCURACY:	±.2 dB DC TO 1.5 kHz (SEE ERROR PLOT)
FREQUENCY ACCURACY:	±2%
RC TEMPERATURE COEFFICIENT:	300 ppM/°C
INPUT IMPEDANCE:	10 kΩ MINIMUM
OUTPUT IMPENDANCE:	50 Ω
MAX INPUT VOLTAGE:	±10 VOLTS PEAK
MAX OUTPUT VOLTAGE:	±10 VOLTS PEAK
MAX OUTPUT CURRENT:	±5 mA PEAK
POWER:	±15 V @ 75 mA/CARD (8 FILTERS)
DC DRIFT:	±20 μV/°C (TYPICALLY)
TEMPERATURE RANGE:	0 – 50°C
PACKAGE:	8 OF THE FILTERS ARE PACKAGED ON A SINGLE PC BOARD WHICH WILL PLUG-IN A CARD SLOT FOR AN AUGAT 8136-RG4 PLUG-IN PC CARD.

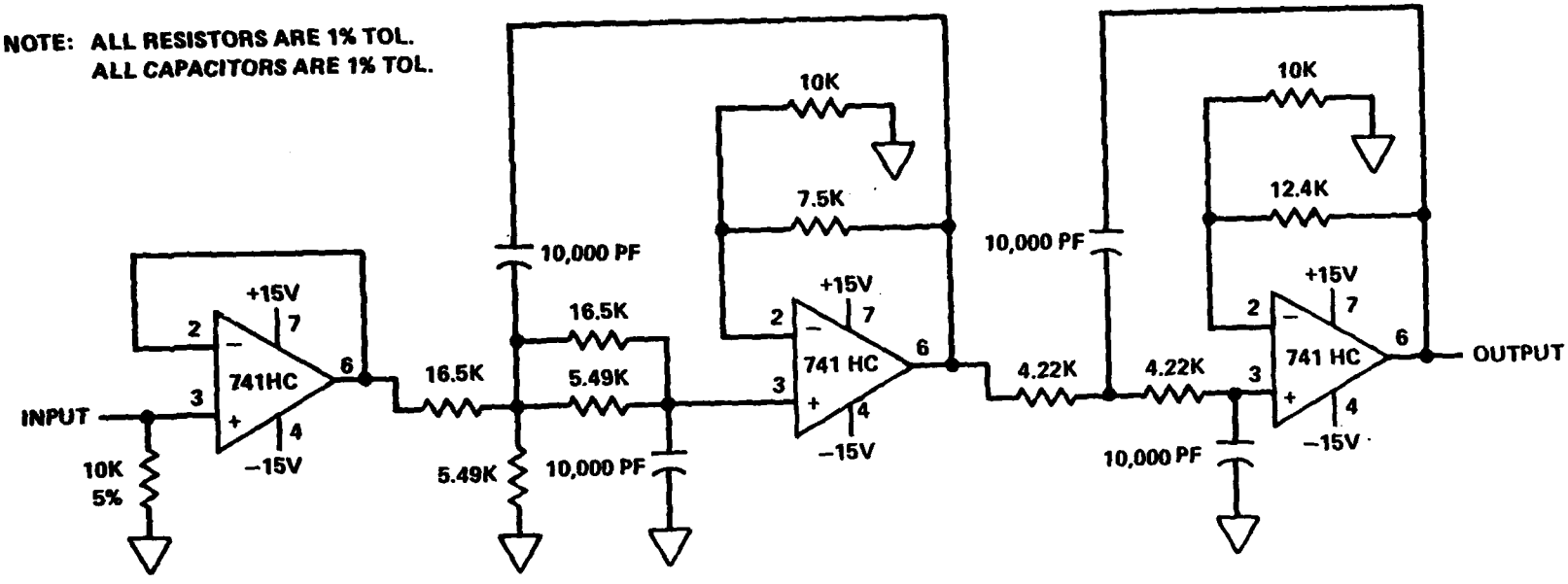

FIGURE G-1 $1\frac{\text{SIN X}}{\text{X}}$ FILTER (8 FILTERS PER CARD)

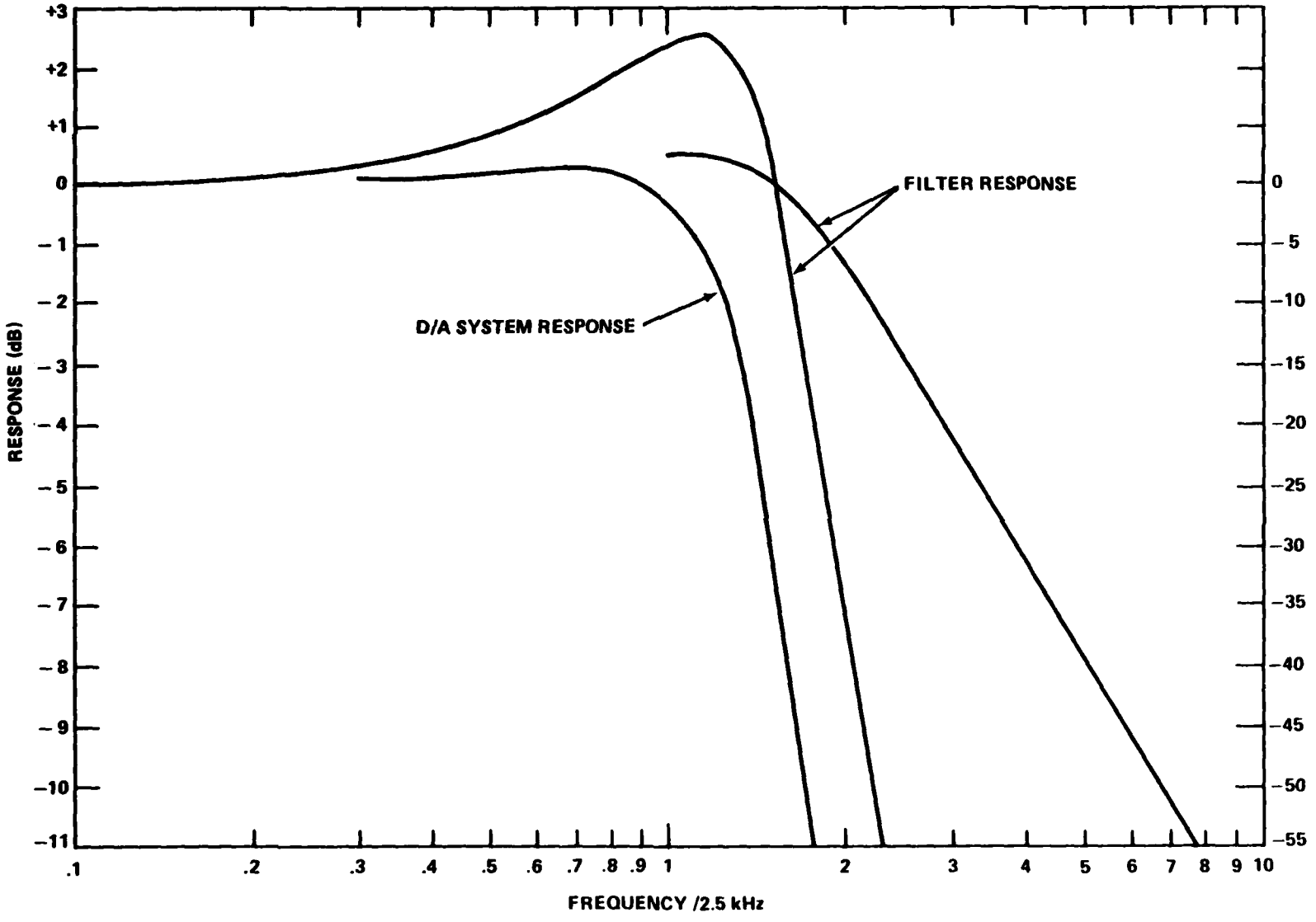

FIGURE G-2 FREQUENCY RESPONSE OF D/A OUTPUT FILTER

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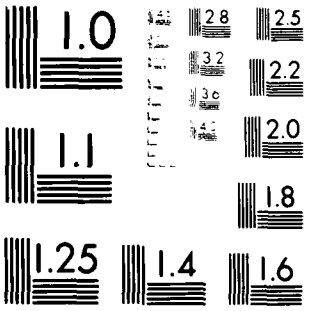

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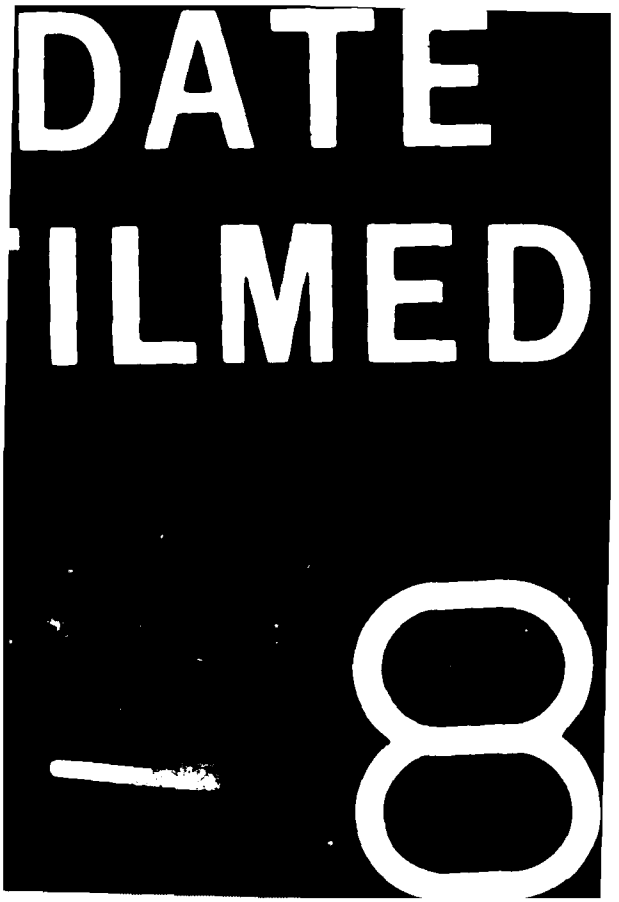
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